Implementation of IEEE 1687 Standard for Access Instrumentation Using Verilog

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Abstract— Technology in VLSI industry has improved in accordance with moore’s law, so density of transistor in Integrated Circuit(IC) is increased. Testing this IC with the bed of nail technique becomes very difficult so solution to this was given by IEEE 1149.1 boundary scan standard also called as Joint Test Access Group(JTAG) using which interconnects between the IC mounted on PCB was tested without physical access. The JTAG Test Access Port(TAP) was used for additional purposes in industry to access the embedded instruments within in the semiconductor device so to standardize the method to access, test, debug, configure and monitor IEEE 1687 standard was developed. This IEEE 1687 standard also called as Internal test Access Group(IJTAG). In this paper the IEEE 1687 is implemented in verilog and simulated in Xilinx 13.1 ISE sim and synthesized using RTL complier in 180nm technology library.

Keywords— Bed of nail, IEEE standard 1149.1, TAP, IEEE 1687 standard

I. INTRODUCTION

The advancement in semiconductor industry has made it conceivable to place numerous Integrated Circuit(IC) on the Printed Circuit Board(PCB). In recent times the Ball Grid Array(BGA) packaging technique is used for IC that is placed on PCB because of physical space constrain. Along with the advantage provided by BGA, this packaging style also have several disadvantages like loss of physical access to the signals so testing of these IC using bed of nails technique was very difficult. The IEEE 1149.1 [1] standard commonly known as Joint Test Access Group (JTAG) or boundary scan architecture along with Test Access Port (TAP) provided a solution for above problem. Initially boundary scan was used to test the interconnects between the IC mounted on PCB without physical access as shown in Figure 1. Later JTAG TAP was also used in ad hoc manner in industry to access the internal core logic as shown in Figure 2, but the problem was to access the embedded internal core logic from different level. The companies found solution i.e. using IEEE 1500 [2].Using IEEE 1500 standard the patterns can be brought from inside the core logic to the boundary of Intellectual Property(IP) as shown in Figure 3, but the problem remains user has access to only the top level Tap ports this is where the user has to define the care and control bits. In the end it the problem of the user to bring

Figure 1 JTAG Architecture to Test the Interconnects Between Core [4]

Figure 2 JTAG Architecture To Access The Core Logic [4]
So the IEEE 1687 standard [3] was developed to standardize the method of accessing the IP from different levels. The IEEE 1687 standard as shown in figure 4 allows the user to define the care bits at where it belongs and it is the responsibility of the application tool to bring the care bits to top level. The IP which is IEEE 1687 compliant is called instruments. Examples of instruments are built-in self test (BIST), phase lock loop (PLL). This IEEE 1687 standard also called as internal test access group (ITAG), the IEEE 1687 provides flexibility and the length of the scan chain can be made variable by using segment insertion bit (SIB). Using this SIB reduces the engineering time and memory.

The hardware architecture of IEEE 1687 standard is shown in Figure 5. It consists of JTAG TAP controller on the left, instrument on the right and 1687 access network in between the TAP and instrument. The 1687 network has two interfaces namely host interface and client interface. The host interface of access network interacts with the client interface of the instrument and client interface of access network interacts with the controller.

A. TAP Controller

The TAP controller as shown in figure 6 has four input Test Mode Select (TMS), Test Data Input (TDI), Test Data Output (TDO), Test Clock (TCK) pins are connected to the chip pin. The TAP controller generates many signals using which the access network can be operated. The signal generated by TAP controller are listed in table 1.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Width</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ScanIn</td>
<td>1</td>
<td>Output</td>
<td>Serial data input</td>
</tr>
<tr>
<td>ScanOut</td>
<td>1</td>
<td>Output</td>
<td>Serial data output</td>
</tr>
<tr>
<td>CaptureEn</td>
<td>1</td>
<td>Output</td>
<td>It allows the shift storage element to collect data from parallel inputs</td>
</tr>
<tr>
<td>ShiftEn</td>
<td>1</td>
<td>Output</td>
<td>It causes the shift operation in serial scan chain</td>
</tr>
</tbody>
</table>
| UpdateEn   | 1     | Output    | It causes the update storage elements to copy data from shift storage element and...
B. Test Data Register (TDR)

The IEEE 1687 network contains TDR’s which has scan mux elements for network control and configuration and also has instrument interface element to control and observe the instruments as shown in figure 7. Five different modes in which TDR can operate is Write only TDR, Read only TDR, Read-Write TDR, Read Write TDR that allows functional access. Read Write TDR bit with control signals.

<table>
<thead>
<tr>
<th>TCK</th>
<th>Input</th>
<th>Capture, Shift &amp; update are synchronized with test clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>Select</td>
<td>1</td>
<td>Output</td>
</tr>
<tr>
<td>Reset</td>
<td>Output</td>
<td>It will reset the update storage elements to reset values</td>
</tr>
</tbody>
</table>

\[Figure 7 Test Data Register [3]\]

C. Segment Insertion Bit (SIB)

The IEEE 1687 network contains Segment Insertion Bit (SIB) accessing an alternate scan chain is shown in figure 8 using which the length of the scan chain can be made variable length. When SIB is asserted the register behind SIB can be accessed and the shift and update operation is conducted and enables the instruments control signals and scan chain length is increased. When SIB is deasserted and disables the instruments behind it.

\[Figure 8 Segment Insertion Bit [3]\]

When select is high and shift is high. The value in the scanout_in is taken which is output of TDR connected to SIB. The value from scanout_in is shifted out and it is available at Scan out as shown in figure 9.

\[Figure 9 SIB when Shift is high and select is high[3]\

When select is low and shift is high the Scan In value is taken and it is shifted because the shift is high and it is shifted out to Scan out as shown in the figure 10.

\[Figure 10 SIB when Shift is high and select is low[3]\

When and shift is low and update is high as shown in the figure 11 the value present in the shift cell is shifted out and it is updates at the negedge of clock to the Select_out which is input to the TDR. If the value of the Select_out is high then the instrument behind the TDR is selected and length of the scan chain is increased if the value of the Select_out is low then the instruments is not selected it is bypassed and the length of the scan chain is reduced.

\[Figure 11 SIB when Shift is low and update is high[3]\

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1. SIB operates in three different modes when select is high and shift is high. The value in the scanout_in is taken which is output of TDR connected to SIB. The value from scanout_in is shifted out and it is available at Scan out as shown in figure 9.
2. When select is low and shift is high the Scan In value is taken and it is shifted because the shift is high and it is shifted out to Scan out as shown in the figure 10.
3. When and shift is low and update is high as shown in the figure 11 the value present in the shift cell is shifted out and it is updates at the negedge of clock to the Select_out which is input to the TDR. If the value of the Select_out is high then the instrument behind the TDR is selected and length of the scan chain is increased if the value of the Select_out is low then the instruments is not selected it is bypassed and the length of the scan chain is reduced.
III. RESULTS

The results of both IEEE 1687 standard is discussed here. The power, area is taken using cadence tool.

A. IEEE 1687 standard result

The first TDR is connected to the asynchronous counter instrument. CLK and RST of the asynchronous counter is mapped with the main clk and rst and the output of the asynchronous data is given to data_out of the TDR. The second TDR is connected to the memory element. Along with clk, rst input the memory also requires other two inputs like addr and we which is applied at the top level and the data_in required for the memory is taken from TDR output and the memory output is given to the TDR. The third instrument is digital clock and it has two inputs clk and rst which is taken from the top level and it has three outputs. The three outputs are seconds, minute, hour. All the three outputs are given to different TDR and it is connected to top level via SIB.

The simulation results of IEEE 1687 standard is as shown below. The clk, rst, scan_in, shift, capture, update, we, addr[3:0] is applied from the top level. The output of first instrument is shown in the figure 12. The second instrument memory output is shown in figure 13. The output of first instrument is shown in the figure 12. The second instrument memory output is shown in figure 13. The output of the third instrument digital clock seconds minutes hour output is shown in figure 14 and scan_out of SIB is the connected to main scan_out which the main output and it is shown in figure 15.

IV. CONCLUSION AND FUTURE WORK

The IEEE 1687 which is effective way to access the embedded instruments using the TAP controller of
1149.1 standard. Along with the advantage of IJTAG it also causes security problem because anyone who can shift the data in the scan chain can access the embedded instruments and obtain the important information like chip ID which is not advisable. So, In future work the security can be provided to the IEEE 1687 standard.

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REFERENCE


