ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 9, September 2017

VHDL Design of Low Power Circuit Employing Clock Gating Technique

[1] Akshat Singh
[1] Department of Electronics and Communication Engineering,
Vaish College of Engineering, Rohtak 124001, India

Abstract:-- **With continuous increase in number of transistors placed on single chip and continuous decrease in minimum feature size of transistors has led to significant increase in device density and device complexity at cost of power demand, has brought need of power optimization in such chips with most common implementation in VLSI (Very Large Scale Integration) circuits. VLSI circuits are both combinational and sequential circuits in nature. But in case of sequential circuits, clock is major source of power consumption. This paper proposes Clock Gating technique to decrease clock power consumption by cutting off ideal clock cycles. Here, a VHDL based technique is used to insert clock gating circuit and dynamic power is calculated and thereafter, model has been implemented onto ISCAS'89 benchmark circuit compiled by Modalism Alters 13.1 and Xilinx ISE tool for simulating and analyzing power and results obtained revels that dynamic power is reduced for sequential circuits.**

Index Terms **— Clock Gating, Low Power, Sequential Benchmark Circuit, VLSI**

I. INTRODUCTION

In recent years, Simultaneous Wireless Information and Power Transfer (SWIPT) has received an upsurge of For modern integrated circuit designs power consumption has become a major concern, with the decrease in feature sizes and increase in clock frequencies. While working on low-power designs, five top most reasons for wasted power are shown in Fig.1 [1]. For design optimization, VLSI designer must work on three performance parameters i.e. Area, Power, and Speed. In order to satisfy the demands of today's consumer i.e. more functionality, high speed, small size, and optimized power devices, one has to minimize power at each levels. The simplest technique to optimize power is by cutting down the clock supply for those blocks of the sequential circuit under which it stays in idle state or not in use for long period [2]. In a digital circuit power consumed is of two types:

(1) Static power
(2) Dynamic power.

Power dissipated because of leakage currents is known as Static power while power dissipated because of switching of active components i.e. capacitor is known as Dynamic power. For the synchronization of active components in VLSI circuit, clock signals are used. The main component of the power in VLSI circuits is clock power as it is supplied to most of the circuit components, and it switches every cycle, which proves that the total clock power is a substantial component of total power dissipated in a digital circuit [2]. Before optimizing power, one must know about the amount of the power the circuit must be dissipating while considering its application. Thus for power optimization, one must work in the direction to reduce the switching capacitance that occurs in the clock network and also the switching activity because of these storage elements during the idle clock states [3]–[4]. In general, switching power is 70%-90 % of power dissipated [5]–[6]. For analysing the speed performance, the average power dissipated (switching activity of the circuits) [7]–[8]. For limiting the switching activity in VLSI Design, idle cycles of flip flop are cut down by the clock gating technique in synchronous circuits [9]–[10].

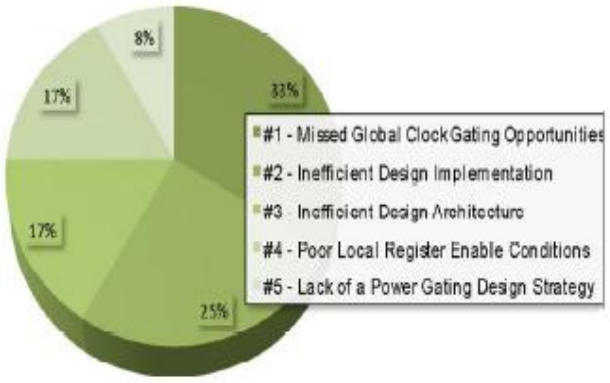

Fig.1. 5 most reasons for wastage of power

In this paper, VHDL based technique is used to insert clock gating circuit and dynamic power is calculated and thereafter,

All Rights Reserved © 2017 IJSEM

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 9, September 2017

model has been implemented onto ISCAS'89 benchmark circuit compiled by Modelism Alters 13.1 and Xilinx ISE tool for simulating and analyzing power and results obtained revels that dynamic power is reduced for sequential circuits. The remaining portion of this paper comprises of Section 2, which explains the clock gating techniques; Section 3 explains the design of D flip flop using clock gating technique; Section 4 explains the power analysis of D flip flop Section 5 explains the experimental results; Section 6 concludes the paper; and Section 7 marks the references used in this paper.

II. CLOCK GATING

The procedure to select required portion of wave in between specified time intervals or specified amplitude limits is clock gating so that average power dissipated or switching activity of the circuits can be limited is known as clock gating. It utilizes combinational logic components for the signal by controlling. In other words, clock gating is the method of addition of extra logic for driving the gated clock which is supplied to the D flip flop. Further, Clock gating is the power optimizing technique because it minimizes the power at gate level, register transfer level (RTL) and system level. We achieved higher levels of power optimization in RTL level than gate level as operations in register transfer level (RTL) are carried out by register blocks while operations in gate level are carried out by logic gates. The main operation of the clock gating technique is to cut down the clock during the idle cycles or unused cycles of flip flop [11]. Clock gating can be implemented by using three different types of cell:

(1) Latch based cell
(2) Flip flop based cell
(3) Gate based cell.

In this section, we will limit our discussion to Gate based cell Clock gating technique using AND gate and NOR gate. AND gate is one of the most common gate configuration used as it possesses simple logic shown in Fig.2 [12]–[14]. For clock gating, a two input AND gate is cascaded with four bit counter with one input as clock signal (CLK) and other as enable signal (EN). When enable signal (EN) is equal to logic 0 and clock signal (CLK) take any value (either positive cycle or negative cycle). Output of the AND gate is known as the gated clock (GCLK) and it comes out be logic 0. When enable signal (EN) is equal to logic 1, gated clock (GCLK) varies according to the clock signal (CLK). Further, when gated clock (GCLK) undergoes a transition from high to low (negative edge triggering), counter is incremented. But this technique is not suitable for the positive edge triggering (when gated clock (GCLK) undergoes a transition from low to high) because when clock signal (CLK) is at rising edge and enable signal (EN) goes from logic 1 to logic 0, a glitch arises due to higher falling time period of enable signal (EN) and it leads to hazard (incorrect output). Hence, any hazard generated when enable signal (EN) is equal to logic 1 is directly marked on to the gated clock (GCLK), which specifies the unstable behaviour of this circuit.

Similarly, NOR gate configuration can be designed, which gives gated clock (GCLK) equal to logic 1 if and only if both enable signal (EN) and clock signal (CLK) are equal to logic 0. Thus, enable signal (EN) is supplied through a NOT gate before being passed as one of the inputs of the NOR gate so as to get gated clock (GCLK) when enable is logic 0 and which makes it suitable for positive edge triggered circuits shown in Fig.3 [14]–[15].

Fig.2. Clock gating using AND gate Circuit

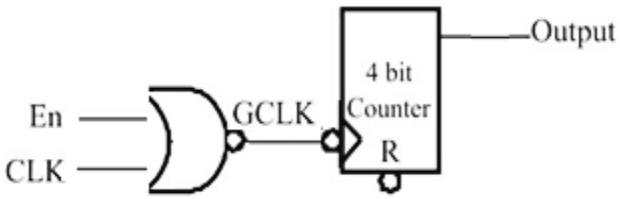

Fig.3. Clock gating using NOR gate Circuit

III. D FLIP FLOP DESIGN USING CLOCK GATING

The most commonly used flip flop for designing of any circuit is the D flip flop because of its simple functioning. The input, which is passed as the input to the D flip flop will appears as output after the clock edge is triggered. It's most commonly application involves memory element as it confirms that the inputs S and R will never be equal to logic 1 simultaneously. To get positive edge triggered D flip flop, output is held until next positive edge is triggered which is the designing principle. On observing the present and next state of the D flip flop, we come to point that when two continuous inputs are similar, the D flip flop gives similar value to that of output. The design of clock gated D flip flop

All Rights Reserved © 2017 IJSEM

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 9, September 2017

is shown in Fig. 4. Here, clock cycle is passed through D flip flop when the output is not varying is defined as idle clock cycles. For removing these, when flip flop is possessing different values, two-input EXOR gate generates logic 1 which is supplied to two-input AND gate as one of input and other being clock pulse signal CLK supplied for getting further switching activity during different cycles of the clock pulses.

The optimized waveform we get for the clock gated D flip flop is shown in Fig 5. Whenever the D and Q values are not equal, EXOR gate is set. To obtain gated clock, EXOR gate output and CLK as an input is passed through AND gate, which generates GCLK signal (gated clock) and it is supplied to input of D flip flop. Further, designed circuit has less number of cycles in comparison to the original clock.

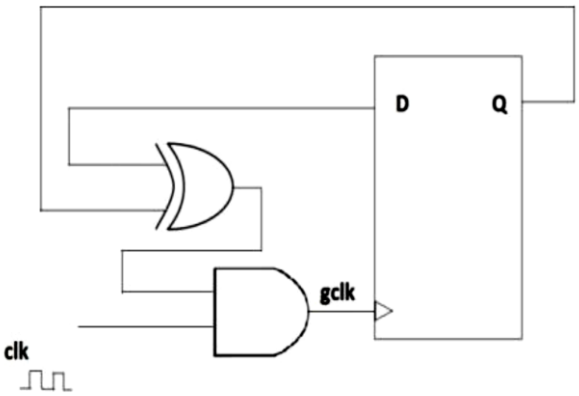

Fig.4. Clock gated D flip flop

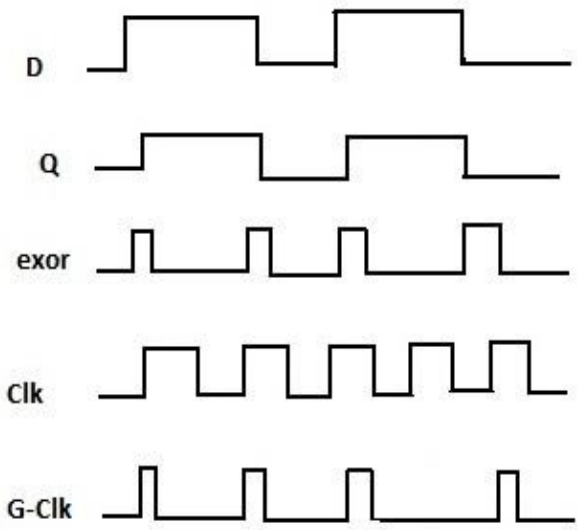

Fig. 5. Waveform for gated D flip flop

IV. POWER ANALYSIS OF D FLIP FLOP DESIGN

For carrying out the power analysis of the D flip flop, we use Xilinx tool in which, VHDL code for the D flip flop is programmed using behavioural model and is simulated in MODELSIM. Under this configuration, we generate generic and package statements that help in managing large design. As the number of cycles in clock gated D flip flop is reduced, the power consumed by the clock gated D flip flop also gets reduced and is compared with original D flip flop as shown in Table 1.

Table 1: Power analysis of D flip flop

Power in absence of Clock Gating	Power in presence of Clock Gating	Power Reduced (% Reduction)
491.70 mW	345.10 mW	146.60 mW (29.81%)

For this analysis, steps involved are
1) A VHDL code with test bench is written and compiled for D flip flop circuit both with clock gating and without clock gating logic in MODELSIM.

2) It is then simulated to obtain the waveform of the circuit and the switching activity of the circuit is monitored by

All Rights Reserved © 2017 IJSEM

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 9, September 2017

creating the VCD file with the help of MODELSIM simulator.

3) The VHDL code is then synthesized in the Xilinx software in order to create NCD file. To analyse power the NCD file and the VCD file is loaded and the dynamic power for the circuit at V CC is at 1.2 V will be calculated by the tool.

V. RESULTS

On carrying out similar steps as depicted earlier, we implement this design for each of the ISCAS'89 benchmark circuits mentioned below, in the MODLESIM tool. In Table 2, the total power of the circuit in the absence of Clock Gating and the total power of the circuit in the presence of Clock Gating has been compared and the power reduced and percentage reduction has been obtained. From this table we found that for higher benchmark circuits the percentage of power reduction is decrease because of area trade-off of the clock gating circuit.

Table 2: Power analysis of benchmark circuits

Circuit	Power in the absence of Clock Gating	Power in the presence of Clock Gating	Power Reduced (% Reduction)
4-bit Counter	2291.8 mW	1788.3 mW	503.5 mW (21.97%)
s27	532.5 mW	327.6 mW	204.9 mW (38.48%)
s298	2405.1 mW	1370.5 mW	1034.6 mW (43.02%)
s444	2750.05 mW	1558.05 mW	1192 mW (43.34%)
s838	15280.3 mW	14539.1 mW	741.2 mW (4.85%)
s1196	105630.7 mW	104470.4 mW	1160.3 mW (1.09%)

CONCLUSION

In research field of VLSI design, problem of power consumption has become major concern since the decrease in feature sizes and increase in clock frequencies. Clock gating technique proposed in this paper is designed on the basis of relationship between the clock transition and present and the next state function of the flip flop. The dynamic power is minimized by cutting down the idle clock cycles of the flip flop by disabling input supplied to clock. Thereafter, power was calculated by using Spartan 3 FPGA family for different clock gated benchmark circuits and from obtained results we came to conclusion that power consumption has been reduced but there is an area trade off concern.

Proposed model is compatible with almost every circuit and can be implemented in smart grid circuit, it is found that these are efficient for logical integration of number of input-output configurations based on the need and specification of circuits.

REFERENCES

[1] P.G. Kaushik, S.M. Gulhane, and A.R. Khan, "Dynamic Power Reduction of Digital Circuits by Clock Gating," International Journal of Advancements in Technology (IJAT), vol. 4, no.1, pp. 79-88, March 2013.

[2] M. Shelke, and B. Humane, "Low Power VLSI Design using Clock-Gating Technique," International Journal of Advanced Research in Computer Engineering & Technology (IJARCET), vol. 4, no.7, pp. 3270-3274, July 2015.

[3] D.K. Sharma, "Effects of Different Clock Gating Techniques on Design", International Journal of Scientific & Engineering Research (IJSER), vol. 3, no.5, pp. 1-4 May 2012.

[4] J. Shinde, and S.S. Salankar, "Clock Gating – A Power Optimizing Technique for VLSI Circuits", India Conference (INDICON), Annual IEEE, December, 2011

[5] N. R. Prakash, and Akash, "Clock Gating for Dynamic Power Reduction in Synchronous Circuits", International Journal of Engineering Trends and Technology (IJETT), vol. 4, no. 5, pp.1760-1763, May 2013.

[6] M. Asyaeia, A. Peiravi, "Low power wide gates for modern power efficient processors", Integration-the VLSI journal, vol. 47, no.2, pp. 272–283, March 2014.

[7] M. Alioto, and G. Palumbo,"NAND/NOR Adiabatic Gates: Power Consumption, Evaluation and Comparison Versus the Fan-In", IEEE transactions on circuits and systems, fundamental theory and applications, vol. 49, no. 9, September 2002.

[8] S.H. Weng, Y.M. Kuo, and S.C. Chang, "Timing Optimization in Sequential Circuit by Exploiting Clock-Gating Logic", ACM Transactions, article. 16, vol. 17, no.2, 15 pages, April 2012.

All Rights Reserved © 2017 IJSEM

[9] Q. Wu, M. Pedram, and X. Wu, "Clock-Gating and Its Application to Low Power Design of Sequential Circuits", IEEE transactions on circuits and systems, Fundamental theory and applications, vol. 47, no. 103, pp. 415-420, March 2000.

[10] E.G. Friedman, "Clock distribution design in VLSI circuits-An overview", Circuits and Systems, ISCAS '93, IEEE International Symposium, May 1993.

[11] N. Srinivasan et al., "Power Reduction by Clock Gating Technique", Science Direct, Procedia Technology, Elsevier vol. 21, pp. 631-635, August 2015.

[12] F. Emnett, M. Biegel, "Power Reduction through RTL Clock Gating", SNUG San Jose, 2000.

[13] G.K.Yeap, "Practical Low-Power Digital VLSI Design", Kluwer Publishing, 1998.

[14] J.F. Wakerly, "Digital Design Principles and Practices", Prentice Hall, 2005.

[15] H. Kaeslin, "Digital Integrated Circuit Design from VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.

All Rights Reserved © 2017 IJSEM