

# PI And P+Resonant CSI Voltage Regulator

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**Abstract**—Recently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Current source inverters offer advantages of voltage boost, short circuit protection, reduced EMI and direct regeneration. While CSI control strategies are less developed than for a VSI, the topologies are functional duals and have much in common in a control sense. The energy performance of various types of voltage source and current-source converters is examined. The VSI has been widely investigated for optimum operation, but the CSI has not been so well studied. A major limitation for the CSI is the availability of modulation strategies with the sophistication and performance of their VSI counterparts. In particular, since CSI voltage regulation is the dual of VSI current regulation, current regulation control strategies for a VSI can be readily implemented as equivalent voltage control strategies for a CSI. The classical PI controller under the fundamental synchronous reference frame can obtain good waveforms under linear load conditions. This paper shows how a high performance PI stationary frame and P+Resonant CSI voltage regulator can be analytically designed and optimised, while in particular taking into account the second order response of a CSI filter/load combination

**Index Terms**— CSI, PI controller, regulation, VSI

## 1. INTRODUCTION

Although voltage source inverters (VSI) are by far the dominant topology for power electronic conversion, current source inverters (CSI) do offer some specific advantages in particular applications. These include voltage boost from a lower magnitude input source, implicit output short-circuit protection, significantly reduced electromagnetic interference because of the capacitive voltage filters located directly on the inverter output, and an ability to directly support regeneration when the dc current is provided by an input SCR rectifier. Hence, CSIs can be useful in applications where their advantages outweigh the obvious fundamental CSI disadvantage of dc series inductor losses.

While CSI modulation and control strategies are less developed than their VSI equivalents, primarily because of their more limited usage in practice, several PWM and closed-loop voltage regulation strategies have been reported. Furthermore, since the two topologies are functional duals and have much in common in a space vector sense, leading edge VSI modulation and control strategies can often be applied to a CSI without significant modification to achieve a similar performance. In particular, the dual of VSI current regulation is CSI voltage regulation. Thus, it could be expected that the advanced current regulation strategies that have been developed for a VSI, such as hysteresis, synchronous frame DQ, stationary frame P+Resonant, and predictive control, can be directly applied to create equivalent CSI voltage regulation strategies.

However, from a control perspective, a VSI is a first-order system, while a CSI is a second-order system with a low-frequency resonant peak caused by the output filter/load network. Hence, strategies used to set controller gains for a VSI are not necessarily directly applicable to a CSI. Furthermore, it is often suggested in the literature that the resonant effect of a second-order system must be mitigated using compensation techniques such as active damping, to ensure system stability under all operating conditions. Optimizing the gains of a system with such an additional feedback path is more complex than for a simple first-order VSI closed-loop regulator, and needs additional investigation.

Although modulation and control strategies for a CSI are much less developed than for a VSI, some advances have been made in applying pulsewidth modulation (PWM) theory to the control of these inverters. More recent work has also shown that, while the two topologies are not exact duals, they do have much in common in a space-vector sense and, hence, modulation strategies that are optimized for a VSI can be applied to a CSI with little modification to achieve similar harmonic benefits.

The primary approach presented in this paper is to use a simple stationary frame proportional-integral (PI) ac voltage regulation strategy for a CSI, since recent work has shown how this approach can be very effective for VSI current regulation once sampling/transport delays and back-EMF disturbance effects are taken into account. Using the principles developed in this work, a strategy is proposed in this paper to optimize controller PI gains for a

CSI, and the performance of the resulting system is then compared against the more advanced P+Resonant regulator to determine its range of effectiveness. Finally, the concepts are applied to a system where active damping has been included as a means of further improving system stability. The results of this analysis show that when controller gains are set to their maximum possible values, active damping offers little or no additional benefit to either controller performance or stability margins.

The most widely used PWM schemes for three-phase voltage source inverters are carrier-based sinusoidal PWM and space vector PWM (SVPWM). There is an increasing trend of using space vector PWM (SVPWM) because of their easier digital realization and better dc bus utilization.

## 2. MODELING A THREE-PHASE CURRENT SOURCE INVERTER CONTROLLED BY A SIMPLE PI CONTROLLER

### Review Stage

Fig. 1 shows the structure of a voltage-controlled CSI, where the switching converter system feeds into an RL load with a back EMF, connected in parallel with the (mandatory) output filter capacitor C. This structure provides a generic representation of most types of three-phase current fed ac load systems, unless there is significant unbalanced cross coupling between the phase load elements.

The CSI voltage regulation control system operates by comparing the measured output voltages against target reference commands. These errors are then used to generate modulation signals which are transformed into VSI space vector switching commands using standard PWM strategies. Finally, the space vectors are mapped to equivalent CSI space vectors and then to device switching signals. (This approach avoids having to develop a separate CSI PWM strategy.)

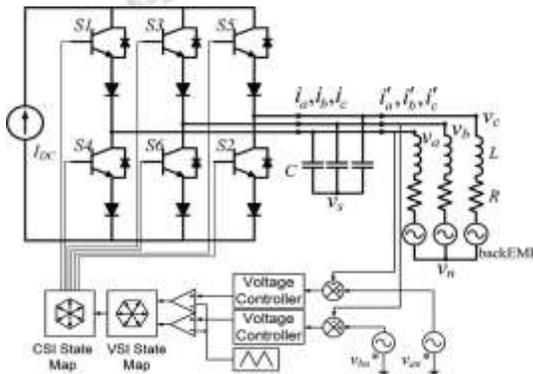


Fig. 1. Three-phase voltage-controlled CSI

Since the focus of this paper is the voltage regulation response, which is significantly slower than the converter switching frequency, the PWM modulator can be modeled as a simple linear amplifier with a gain of  $I_{dc}$ . Essentially, this means that over any particular PWM half-carrier cycle, the CSI modulator can command any required current from each phase leg, provided that the sum of the three-phase leg positive peak current magnitude is less than  $I_{dc}$ . It should be noted that this gain is independent of the PWM strategy used, since the maximum possible output current per phase leg is always  $I_{dc}$  irrespective of the modulation process.

Only two independent voltage regulation loops are required for this system, based on the following analysis. Defining the load star point voltage as  $v_n(t)$ , the relationship between the RL load phase currents  $i'_a(t)$ ,  $i'_b(t)$ ,  $i'_c(t)$  and the converter output voltages is given by

$$v_{an}(t) = Ri'_a(t) + L \frac{di'_a(t)}{dt} + emf_a(t) \quad (1a)$$

$$v_{bn}(t) = Ri'_b(t) + L \frac{di'_b(t)}{dt} + emf_b(t) \quad (1b)$$

$$v_{cn}(t) = Ri'_c(t) + L \frac{di'_c(t)}{dt} + emf_c(t) \quad (1c)$$

KCL constrains the sum of the load currents to be zero, i.e.,

$$i'_a(t) + i'_b(t) + i'_c(t) = 0 \quad (2)$$

Summing (1), substituting from (2), and recognizing that the sum of the three back EMFs must be zero, since they are a balanced three-phase system, identifies that the sum of the converter output voltages must also be zero, i.e.,

$$v_{an}(t) + v_{bn}(t) + v_{cn}(t) = 0 \quad (3)$$

Thus the converter output voltages constitute a balanced three-phase set, as could be expected, and hence, the load star point  $v_n(t)$  is in fact a true zero-voltage neutral point. The CSI output currents for each phase are given by

$$i_a(t) = i'_a(t) + C \frac{dv_{as}(t)}{dt} = i'_a(t) + C \frac{d\{v_{an}(t) + v_{ns}(t)\}}{dt} \quad (4a)$$

$$i_b(t) = i'_b(t) + C \frac{dv_{bs}(t)}{dt} = i'_b(t) + C \frac{d\{v_{bn}(t) + v_{ns}(t)\}}{dt} \quad (4b)$$

$$i_c(t) = i'_c(t) + C \frac{dv_{cs}(t)}{dt} = i'_c(t) + C \frac{d\{v_{cn}(t) + v_{ns}(t)\}}{dt} \quad (4c)$$

where  $v_s(t)$  is the star point voltage of the capacitor filter bank. Once again, KCL constrains the sum of the converter currents to be zero, so that

$$i_a(t) + i_b(t) + i_c(t) = 0 \tag{5}$$

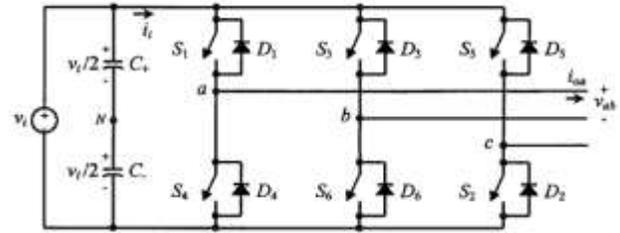
Substituting (2), (3), and (5) into (4) identifies that  $v_{ns}(t) = 0$ , which means that the capacitor network star point  $v_s(t)$  must also be a true zero-voltage neutral point. From this analysis, it then immediately follows that each load phase voltage can be separately and independently controlled by simply regulating the converter current injected into that load/filter phase leg.

Furthermore, since the CSI current reference modulation commands are constrained, it also follows that only two independent voltage regulation loops are required because the third-phase leg current can be directly calculated as the simple inverse sum of the first two-phase leg current references (this is the same concept as the need for only two control loops to control currents in a three-phase VSI). The third-phase leg voltage must automatically follow on to make up a three-phase voltage set because of the current that is forced to flow through it. The CSI voltage regulation requirement, therefore, reduces to creating two-phase current modulation reference signals, determined so as to make their associated load-phase voltages track two regulated phase legs is independent of each other, their controllers will also be independent, and can be considered simply as two separate single-phase systems. Sine-triangle modulation causes the inverter to continuously cycle between these states. For a CSI, there is no direct mapping between the output of a sine-triangle phase leg modulator and the inverter phase legs, because each phase leg can adopt one of three states (either upper or lower or off). Hence an explicit minimum switch criterion must be developed to determine how the three null states of a CSI should be used.

**A. VSI State Map**

The standard three-phase VSI topology is shown in Fig. 2 and the eight valid switch states are given in Table 1. As in single-phase VSIs, the switches of any leg of the inverter ( $S_1$  and  $S_4$ ,  $S_3$  and  $S_6$ , or  $S_5$  and  $S_2$ ) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity. Of the eight valid states, two of them (7 and 8 in Table 1) produce zero ac line voltages. In this case, the ac line currents freewheel through either the upper or lower components. The

remaining states (1 to 6 in Table 1) produce non-zero ac output voltages. In order to generate a given voltage waveform, the inverter moves from one state to another. Thus the resulting ac output line voltages consist of discrete values of voltages that are  $V_i$ , 0, and  $-V_i$  for the topology shown in Fig. 3. The selection of the states in order to generate the given waveform is done by the modulating technique that should ensure the use of only the valid states



**Fig.2. Three phase VSI Topology**

**B. CSI State Map**

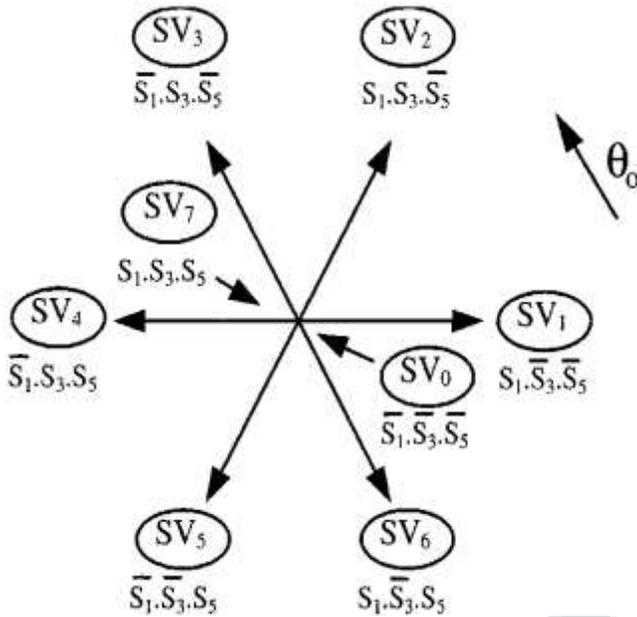
In order to properly gate the power switches of a three phase CSI, two main constraints must always be met: (a) the ac side is mainly capacitive, thus, it must not be shortcircuited; this implies that, at most one top switch (1, 3, or 5) and one bottom switch (4, 6, or 2) should be closed at any time; and (b) the dc bus is of the current-source type and thus it cannot be opened; therefore, there must be at least one top switch (1, 3, or 5) and one bottom switch (4, 6, or 2) closed at all times. Note that both constraints can be summarized by stating that at any time, only one top switch and one bottom switch must be closed.

*Figures*

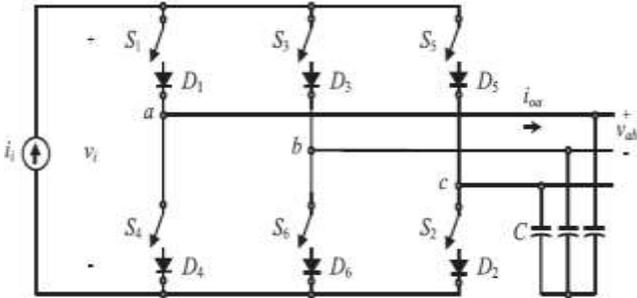
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State	State	$v_{ab}$	$v_b$	$v_c$
1 <sub>1</sub> , 2 <sub>3</sub> , and 4 <sub>6</sub> are on and 4 <sub>4</sub> , 5 <sub>1</sub> , and 3 <sub>5</sub> are off	1	$v$	0	$-v$
2 <sub>1</sub> , 3 <sub>5</sub> , and 1 <sub>4</sub> are on and 5 <sub>3</sub> , 6 <sub>1</sub> , and 4 <sub>2</sub> are off	2	0	$v$	$-v$
3 <sub>1</sub> , 4 <sub>2</sub> , and 2 <sub>5</sub> are on and 5 <sub>3</sub> , 1 <sub>4</sub> , and 5 <sub>6</sub> are off	3	$-v$	$v$	0
4 <sub>1</sub> , 5 <sub>3</sub> , and 3 <sub>5</sub> are on and 1 <sub>4</sub> , 2 <sub>5</sub> , and 6 <sub>1</sub> are off	4	$-v$	0	$v$
5 <sub>3</sub> , 5 <sub>6</sub> , and 4 <sub>2</sub> are on and 2 <sub>5</sub> , 3 <sub>1</sub> , and 1 <sub>4</sub> are off	5	0	$-v$	$v$
6 <sub>1</sub> , 1 <sub>4</sub> , and 5 <sub>6</sub> are on and 3 <sub>5</sub> , 4 <sub>2</sub> , and 2 <sub>5</sub> are off	6	$v$	$-v$	0
1 <sub>1</sub> , 3 <sub>5</sub> , and 5 <sub>6</sub> are on and 4 <sub>2</sub> , 6 <sub>1</sub> , and 2 <sub>5</sub> are off	7	0	0	0
4 <sub>1</sub> , 5 <sub>3</sub> , and 2 <sub>5</sub> are on and 1 <sub>4</sub> , 5 <sub>6</sub> , and 3 <sub>1</sub> are off	8	0	0	0

**Table.1. Valid switch states for a VSI**



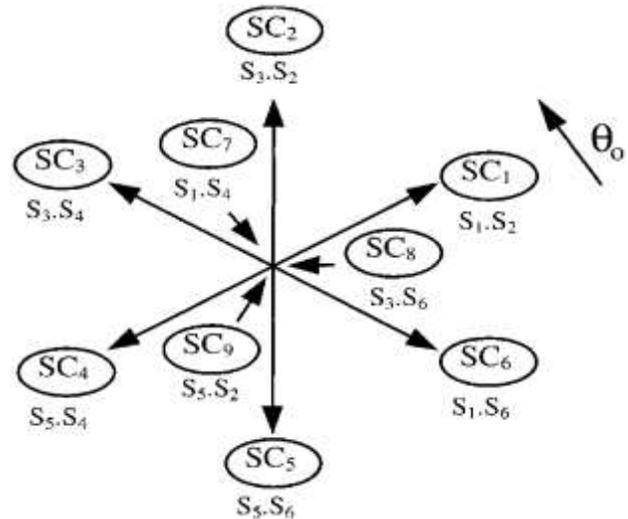
**Fig.3.Space vector states for three phase VSI**



**Fig.4.Three phase CSI Topology**

State	State	a	b	c
1 and 2 are on and 3, 4, 5, and 6 are off	1	1	0	-
2 and 3 are on and 4, 5, 6, and 1 are off	2	0	1	-
3 and 4 are on and 5, 6, 1, and 2 are off	3	-	0	1
4 and 5 are on and 6, 1, 2, and 3 are off	4	-	0	0
5 and 6 are on and 1, 2, 3, and 4 are off	5	0	-	0
6 and 1 are on and 2, 3, 4, and 5 are off	6	-	-	0
1 and 4 are on and 2, 3, 5, and 6 are off	7	0	0	0
3 and 6 are on and 1, 2, 4, and 5 are off	8	0	0	0
5 and 2 are on and 6, 1, 3, and 4 are off	9	0	0	0

**Table.2.Valid switch states of a Three phase CSI**



**Fig.5.Space vector states of three phase CSI**

There are nine valid states in three-phase CSIs. The states 7, 8, and 9 (Table 2) produce zero ac line currents. In this case, the dc link current freewheels through either the switches S1 and S4, switches S3 and S6, or switches S5 and S2. The remaining states (1 to 6 in Table 2) produce nonzero ac output line currents. In order to generate a given set of ac line current waveforms, the inverter must move from one state to another. Thus, the resulting line currents consist of discrete values of current, which are  $i_1$ , 0, and  $-i_1$ . The selection of the states in order to generate the given waveforms is done by the modulating technique that should ensure the use of only the valid states .

**C. MAPPING OF VSI AND CSI STATES**

It should be noted that although the angles between the active space vectors are 60 for both the VSI and the CSI, the CSI active space vectors lead the VSI space vectors by 30 in an absolute sense. Earlier work has shown how the similarity between these two sets of space vectors allows almost any VSI modulation scheme to be used with a CSI simply by mapping the VSI space vectors to the CSI space vectors. This involves taking the VSI phase leg gate signals and mapping them to select the appropriate CSI space vectors. For the active space vectors this is straightforward, as there is a one-to-one correspondence between the VSI and CSI active space vectors. However, the third zero space vector which is available for a CSI means that an additional criterion is required to map the VSI zero states to the CSI.

### 3. DETERMINING THE MAXIMUM PI CONTROLLER GAINS

The target objectives are to maximize the proportional gain  $k_p$  and then to minimize the integrator time constant  $\tau_r$  (maximize the integrator gain), the phase angle of the open loop transfer function (8) at  $\omega_c$  should be set to

$$\angle \{H(j\omega_c) e^{-j\omega_c T_d} I_{DC} G(j\omega_c)\} = -\pi + \phi_m \quad (9)$$

Standard control theory suggests that a suitable phase margin for satisfactory control performance with adequate transient damping is  $40^\circ$ , although the method is suitable for designing any required phase margin in any given system.

The phase angle of (8) is given by

$$\begin{aligned} \angle \frac{V_x(s)}{E_x(s)} &= \angle \left\{ \frac{K_p I_{DC} R (1 + j\omega_c \tau_r) e^{-j\omega_c T_d} (1 + j\omega_c T_p)}{\tau_r j\omega_c (1 - \omega_c^2 LC + j\omega_c RC)} \right\} \quad (10) \\ &= \tan^{-1}(\omega_c \tau_r) - \omega_c T_d + \tan^{-1}(\omega_c T_p) \\ &\quad - \pi/2 - \tan^{-1}(\omega_c RC / (1 - \omega_c^2 LC)) \quad (11) \end{aligned}$$

For most systems,  $\omega_c$  will be well above the plant pole frequency, and hence, the phase contribution of

$$\tan^{-1}(\omega_c T_p) - \tan^{-1}(\omega_c RC / (1 - \omega_c^2 LC)) \text{ is } \approx -\pi/2.$$

Substituting this approximation into (9) and (11) give

$$\phi_m \approx \tan^{-1}(\omega_c \tau_r) - \omega_c T_d \quad (12)$$

$$\omega_c = \frac{\tan^{-1}(\omega_c \tau_r) - \phi_m}{T_d} \approx \frac{\pi/2 - \phi_m}{T_d} \quad (13)$$

$$\omega_{c(max)} = \frac{\pi/2 - \phi_m}{T_d} \quad (14)$$

The maximum possible magnitude of  $k_p$  can now be found by setting the open loop gain at this value of  $\omega_{c(max)}$  to unity

$$K_p = \frac{\tau_r}{R I_{DC}} \omega_c \sqrt{\frac{(1 - \omega_c^2 LC)^2 + (\omega_c RC)^2}{(1 + \omega_c^2 \tau_r^2)(1 + \omega_c^2 T_p^2)}} \quad (15)$$

Finally, the integral time constant  $\tau_r$  can be minimized by making  $\tan^{-1}(\omega_{c(max)} \tau_r) \approx \pi/2$  (say  $85^\circ$ ), which gives

$$\tau_r \approx \frac{10}{\omega_{c(max)}} \quad (17)$$

These gains are the maximum possible that can be achieved while still maintaining an adequate stability margin.

### 4. CSI VOLTAGE REGULATION USING A P+RESONANT CONTROLLER

The analysis presented above allows the maximum possible gains to be analytically determined for a PI regulator to maintain a required stability margin while still achieving the best possible dynamic performance. However, (13) and (14) also show that the overriding limitation on gain is the controller sampling/transport delay  $T_d$ , which is in turn directly dependent on the PWM switching frequency. Hence for a higher power converter with a lower switching frequency, it may just not be possible to get an acceptable (and stable) dynamic performance even when the controller gains are set to their maximum possible values. In such situations, it is necessary to use a controller that can provide significantly increase gain at the target reference frequency without increased higher frequency gain (which would compromise stability), such as a synchronous frame or a P+Resonant controller. For this paper, a P+Resonant controller has been implemented to illustrate the issue. The general form of a P+Resonant controller is given by

$$H_{P+R}(s) = K_P \left( 1 + \frac{1}{\tau_r} \frac{s \omega_o}{s^2 + \omega_o^2} \right) \quad (18)$$

from which it can be seen how the resonant term in the denominator dramatically increases the controller gain at the target frequency  $\omega_o$  without particularly affecting the high frequency proportional gain. The gains of this controller are set to the same values as have already been determined for the simple stationary frame PI controller. For this part of the investigation, the PWM switching frequency was reduced to a low 600 Hz, to greatly exacerbate the phase roll-off of the forward path gain, because of the very large transport delay that occurs at this switching frequency. The resulting frequency and transient step responses for both a simple PI and a P+Resonant regulator, with the gains set to their maximum values for both cases. These results clearly show the benefit that can be achieved using the more sophisticated P+Resonant controller in these low switching frequency conditions.

If the load resonant frequency is set to the target reference frequency, the system provides “free gain” that will improve the steady state and transient performance even for

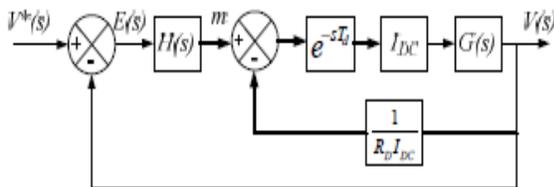
a simple PI regulator. While the resulting performance of the simple PI regulator is still not as good as the P+Resonant system, it is quite acceptable, and is most certainly completely stable without any need for active damping.

### 5. THE ROLE OF ACTIVE DAMPING

To suppress the LC resonance, one of the methods is to connect a physical damping resistor in parallel with the filter capacitor. If the damping resistor is small enough, the LC resonance can be sufficiently damped out, and the drive may be stabilized. Obviously, this method is not practical due to the high energy loss on the damping resistor. To solve this problem, an active damping control is proposed. The equivalent damping current  $i_d$  is obtained by detecting the capacitor voltage and then dividing the voltage by a damping factor  $R_D$ . The damping current is then subtracted from the inverter reference current. When a LC resonance occurs, the damping current which is in phase with the resonant voltage will be subtracted from the inverter output current, and thus the LC resonance is effectively suppressed.

#### A. Selection of Damping Factor $R_D$

The damping factor  $R_D$  is mainly associated with the size of inverter capacitor and switching frequency. The reciprocal of the damping factor is approximately proportional to the capacitor size. The higher the switching frequency, the smaller the damping factor & can be used, and the stronger the damping effect can be gained. A typical approach is shown in Fig. 9, where the additional feedback path is used to smooth out the system resonance. the overall gain of the system reduces, and the controller gains must be retuned to maintain optimal system performance.



**Fig.9. Single Phase voltage regulator with active damping**

$$\frac{V(s)}{V^*(s)} = \frac{G(s)I_{DC}H(s)}{1 + G(s)I_{DC}(H(s) + 1/I_{DC}R_D)}$$

(19)

If the active damping loop is incorporated into system, the expression for the open loop transfer function phase now becomes

$$\phi = \tan^{-1}(\omega_c T_p) - \omega_c T_d - \tan^{-1} \left( \frac{(RC + L/R_D)\omega_c}{1 + R/R_D - \omega_c^2 LC} \right) \quad (20)$$

If the integral time constant remains at the same approximation of  $\tau_r \approx 10 / \omega_c$ . Hence the expression for maximum  $K_p$  with active damping can be expressed as (21).

$$K_p = \frac{\omega_c \tau_r}{I_{dc} \sqrt{1 + (\omega_c \tau_r)^2}} * \frac{\sqrt{(\omega_c RC + L/R_D)^2 + (1 + R/R_D - LC\omega_c^2)^2}}{(\omega_c^2 L^2 + R^2)} \quad (21)$$

There is no doubt that active damping achieves its goal of reducing the system resonant peak. It can be seen that the introduction of active damping has contributed nothing to either the high frequency gain response, or to the stability margin. In fact, its only contribution appears to be to reduce the system load/filter resonance, which has been shown in this paper to actually be potentially advantageous in certain applications. Hence the benefits of including active damping into a correctly tuned PI control system (or a P+Resonant system since the gains are the same) seem at best uncertain, and at worst counterproductive.

### 6. CONCLUSION

- The work presented in this paper shows how PWM transport and sampling delays are a significant factor that must be considered when designing a high performance stationary
- Frame PI or P+Resonant voltage controller for a Current Source Inverter. From this understanding, a deterministic analytical method is presented which calculates the maximum
- possible PI and P+Resonant gains that can be achieved for this system. The controller does not need active damping to maintain stability or improve performance despite the highly
- resonant nature of the plant. The analytical development is supported by detailed simulation

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