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Cascaded Multilevel Inverter Topology with SPWM and Selective Harmonic Elimination Modular Techniques-A Review

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***Abstract*— In the recent decades Multilevel inverters have been attracted the wide interest of researcher as well as industry for high-power and medium-voltage control. Additionally, they can combine switched waveforms with lower levels of harmonic distortion compared with the conventional two-level converter. The multilevel model is used to decrease the harmonic distortion in the output waveform without decreasing the inverter output power. This paper presents the most important popular topologies like diode-clamped or neutral point clamped inverter, flying capacitor or capacitor-clamped inverter, and cascaded H bridge multilevel inverter. Most commonly used modulation technique such as Sinusoidal, Modified and Random Pulse Width Modulation, Third harmonic injection, Space Vector Pulse Width Modulation Technique (SVPWM), Delta Modulation, Selective Harmonic Elimination (SHE) and Wavelet Modulation Technique (WM) are discussed and a review on CCHMLI with most frequently used control techniques such as SPWM and SHE methods are discussed enabling improvement in technology in both industry and research areas.**

***Index Terms*— Multilevel converter (MLC), Diode clamped or Neutral point clamped MLI (NPC or DCMC), Flying Capacitor MLI (FCMC), Cascaded Cell H-Bridge**

I. INTRODUCTION

In the recent years, multilevel inverters are the preferred choice of industry for high voltage and power applications. Multilevel inverter technology has emerged as a very important alternative in the area of high-power medium-voltage energy control. Renewable energy sources such as Solar, Wind, Fuel cells can be interfaced to a multilevel converter system [1,2].Many Research work has been carried out on various converter topologies with the suitable modulation technology to reduce various parameters related to increase its performance. Different types of multilevel converter models are: cascaded H-bridge converter, diode clamped and flying capacitors. Most frequently used control & Modulation architypes have been discussed such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. Many, multilevel converter applications include industrial medium-voltage motor drives, renewable energy systems with utility interface, flexible AC transmission system, and traction drive systems. The common used MLC topologies are the neutral-point-clamped converter (NPC), flying capacitor converter (FC) and Cascade H-Bridge (CHB) have developed over last few decades [3].

Advantages of MLIs

A. Based on the waveform:

- Better quality of waveform in terms of THD
- Better harmonic reduction with reduced number of filter elements.
- Lower dv/dt stress
- Smaller CMVs
- Modulation Techniques are possible at Low and High switching Frequency

B. Based on Topology

- When compared to operating voltage the voltage rating of power switches are less.
- Multiple redundant states
- Load sharing among the inputs sources are equal
- RES can be easily integrated as a source.

II. TYPES OF CONVERTERS:

Figure 1 and 2 depicts the types of DC-AC Converters and types of multilevel inverters respectively.

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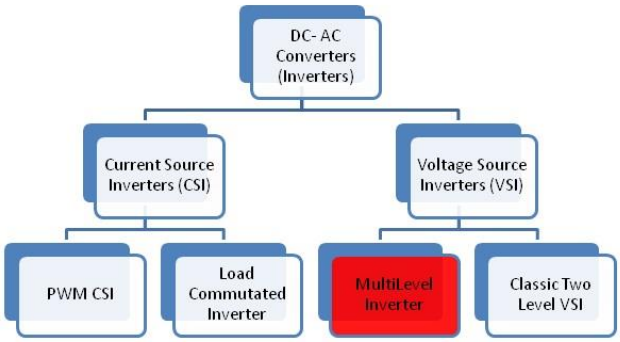

Figure 1:Types of DC-AC Converters

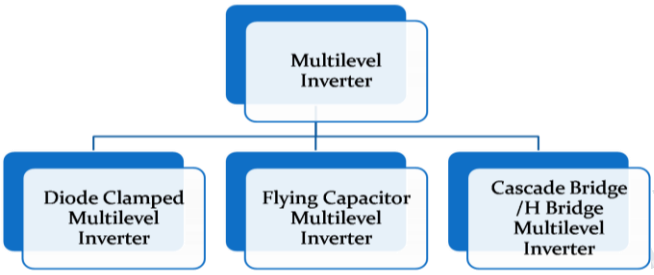

Figure 2: Types of Multilevel Inverters

1. Diode Clamped or Neutral Point clamped multilevel inverter (NPC-MLI)

NPC-MLI are also known as Diode Clamped multilevel inverter was first proposed by Nabae *et. al* in 1980. Figure 3 shows the 3-level NPC inverter.

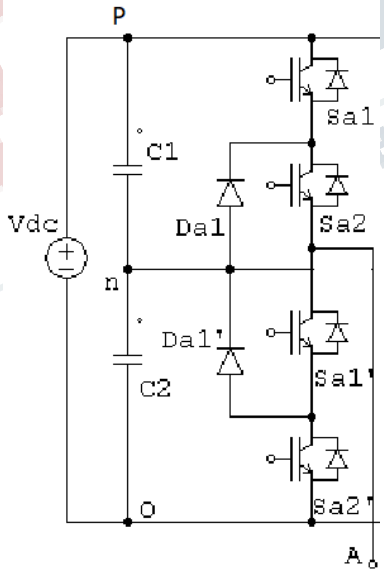

Figure 3: One leg of three-level Neutral-Point-Clamped inverter.

Consider one leg of three-level Neutral-Point-Clamped inverter as shown in the figure 3.The structure has a DC link voltage of V_{dc} which is generally halved using capacitors C_1 and C_2. Each capacitor has $V_{dc}/2$ volts and each voltage stress will be limited to one capacitor level through clamping diodes D_{a1} & D_{a1}'. The output voltage V_{An} has three states: $\pm V_{dc}/2$ and 0.

State 1: When switches S_{a1}, S_{a2} are ON & S_{a1}', S_{a2}' are OFF the potential at A is **+ $V_{dc}/2$**.

State 2: When switches S_{a2}, S_{a1}' are ON & S_{a1}, S_{a2}' are OFF the potential at A is **0V**.

State 3: When switches S_{a1}', S_{a2}' are ON & S_{a1}, S_{a2} are OFF the potential at A is **- $V_{dc}/2$**.

Generally the voltage stress across the power switches is less than the operating voltage. A three phase structure is obtained by adding two more three level legs as shown in the figure 3.1.

An n-level NPC inverter consists of (n-1) capacitors, 2(n-1) switching devices per phase and 2(n-2) clamping diodes per phase. The number of levels can be extended to a higher level by additional more number of switching devices and with these additions [4-5] , the inverter will achieve higher AC voltage, producing more voltage steps with less harmonic distortion nearing to sinusoidal waveform. During inverter operations, the switches near the center tap are switched on for a longer period compared to the switches further away from the center tap. Major difference between the conventional 2-level and multilevel NPC is the clamping diode D_{a1} & D_{a1}'.

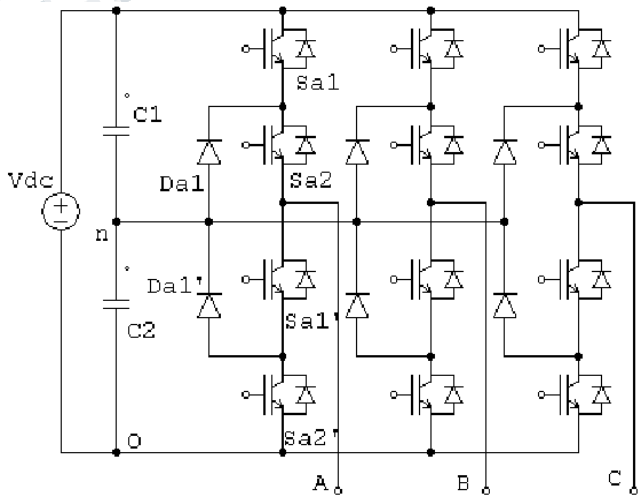

Figure 3.1: Three-level Neutral-Point Clamped inverter.

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Diode clamped inverter has the following advantages as listed below:

- Increasing the number of levels of the inverters harmonic distortions are reduced.
- As the switching frequency is low, constraints on switches are reduced with controlled reactive power flow.
- High efficiency (Fundamental frequency).
- Simple Control methods for a back-to-back Intertie system.

Disadvantages:

- Circuit complexity increases with the increase in the number of levels & clamping diodes.

2. Flying-Capacitor Multilevel Inverter (FC-MLI):

FC-MLI was introduced in the late 1980's.This topology is same as NPC-MLI topology instead of clamping diodes a capacitor-clamping or a flying-capacitor are used to clamp the voltages [6].Capacitors which are not directly connected to the positive or negative DC rails; hence the name "Floating" of "Flying " capacitor topology. The voltage between the two capacitors refers to the output voltage at the terminal [7]. The voltage level in the flying-capacitor inverter is same as like in the diode-clamped multilevel inverter [8].The floating capacitor is "pre-charged" to a voltage $V_{dc}/2$. The modulation scheme has to ensure proper dissemination of voltage across each capacitors.

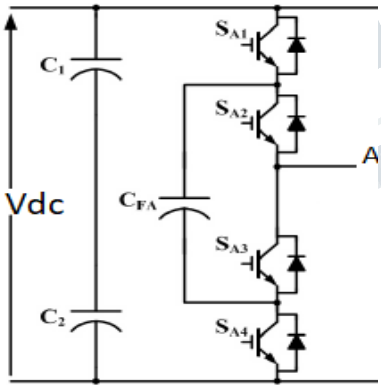

Figure 4: one leg of three-level flying-capacitor multilevel inverter (FC-MLI)

Consider one leg of 3-level FC-MLI as shown in the figure 4 which has output voltage across 'a' and 'n' points such as Vdc/2, 0, (−Vdc)/2. There are four valid states as discussed below.

State 1: When switches S_{A1}, S_{A2} are ON & S_{A3}, S_{A4} are OFF the potential at 'A' is **+ $V_{dc}/2$**.

State 2: When switches S_{A1}, S_{A2} are OFF & S_{A3}, S_{A4} are ON the potential at 'A' is **- $V_{dc}/2$**.

State 3: When switches S_{A1}, S_{A3} are ON & S_{A2}, S_{A4} are OFF the potential at 'A' is **0V.**

State 4: When switches S_{A2}, S_{A4} are ON & S_{A1}, S_{A3} are OFF the potential at 'A' is **0V.**

State 3 and 4, both leads to the potential of 0V, although with the different switching combinations, resulting in the redundant states. These redundant states are used for balancing the capacitor voltage. For n-level FC-MLI (n-1) number of capacitors on a common DC-bus, where n is the level number of the inverter, and 2(n-1) switch-diode valve pairs are used [9]. A three phase structure is obtained by adding two more three level legs as shown in the figure 4.1.

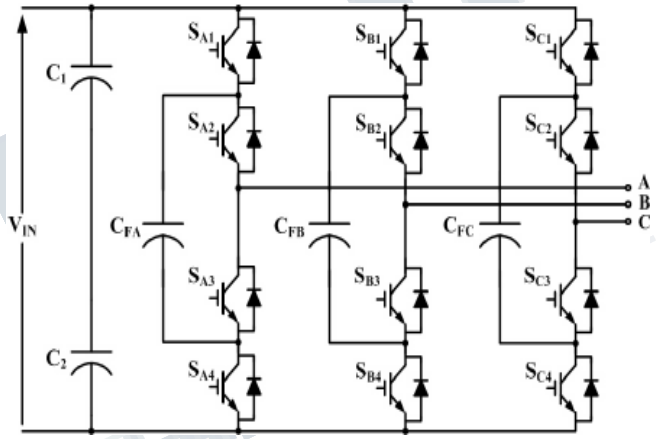

Figure 4.1: Three-level flying-capacitor multilevel inverter (FC-MLI)

3. Cascaded multilevel inverter

The cascaded multilevel inverter or series H-bridge inverter appeared in 1975. Cascaded H-Bridge multilevel inverter are the most advanced and important method of power electronic converters that analyses output voltage with number of dc sources as inputs. Cascaded H-Bridge multilevel inverters requires less number of components and it reaches high quality output voltage which is close to sinewave when compared with the other two topologies [10]. By increasing the number of output levels the total harmonic distortion in output voltage can be reduced. Cascaded H-Bridge multilevel inverter required AC output voltage is obtain by synthesizing number of DC sources such as PV array, Fuel Cells etc.

Lai and Peng, patented and presented its various advantages in the year 1997. Since then, the CMI has been utilized in a wide range of applications. CMI are commonly used in high-power applications, especially shunt and series connected FACTS controllers due to the various modular techniques used.

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By adding more H-bridge converters, the amount of Voltage can simply increase without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized.

Consider one leg of 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vdc, 0, -Vdc (zero, positive dc voltage, and negative dc voltage).There are four different states that exists which are explained below:

State 1: When the switches s_1 & s_2 are turned ON & no source is connected to the load. Output voltage across the load is **Zero.**

State 2: When the switches s_1 & s_4 are turned ON. Output voltage obtained across the load is **+Vdc.**

State 3: When the switches s_2 & s_3 are turned ON. Output voltage obtained across the load is –**Vdc.**

State 4:- When the switches s_3 & s_4 are turned ON. Output voltage across the load is **zero**.

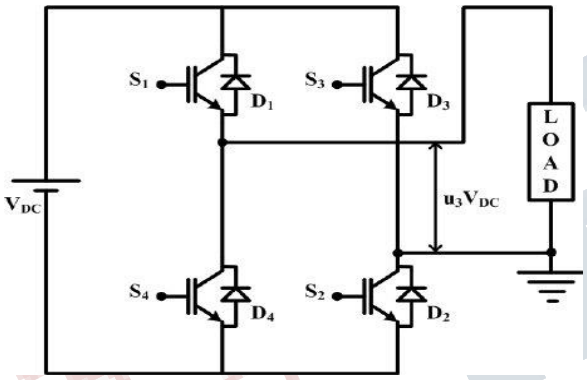

Figure 5 Three-level cascaded inverter for one phase

A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing [11]. Due to this unique feature which is impossible in other VSC topologies utilizing a common DC link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge converter is provided separately. The converter topology is based on the series connection of single-phase inverters with separate dc sources. Figure 5 shows the power circuit for one phase leg of a three-level cascaded inverter. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells.

Advantages

- CMI can be switched at low frequency.
- Modularity of control can be achieved. Unlike the diode clamped and capacitor clamped the full-bridge inverters of a cascaded structure can be modulated separately.
- Number of components required is less compared to other topology for the same voltage levels.
- Suitable for high voltage and high current rating in electric drives.
- Less EMI and voltage unbalance problem.

Disadvantages

- Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.
- Separate dc sources are required for real power conversions with limited applications.

III. MODULATION AND CONTROL STRATEGIES:

There are many types, of modulation techniques available, for simple implementation with improved efficiency in the practical applications. Most modulation techniques for multilevel inverters are adapted from the traditional methods employed for the conventional two-level inverters. Based on the switching frequency they are broadly classified as low and high switching frequency (1-kHz boundary is considered to differentiate between them)

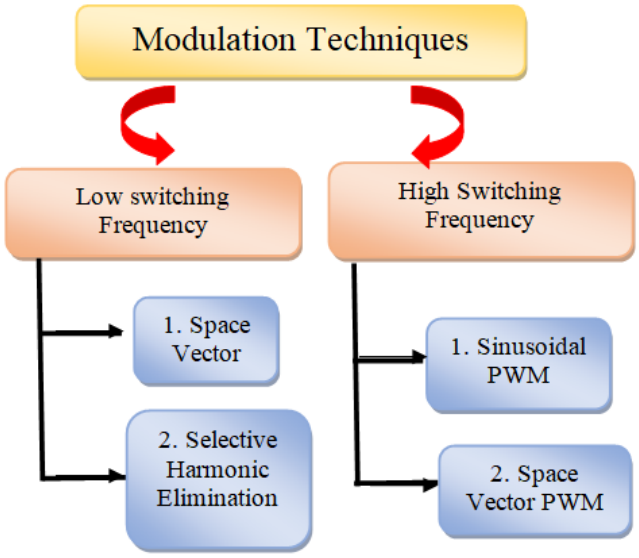

Figure 6: Different types of modulation technique

Low Switching Frequency Methods

Low switching frequency is generally defined to be below 1 kHz.. Low switching frequency methods are generally preferred for high power applications, with reduced switching loss. This method are also effective with more number of voltage levels.

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Selective Harmonic Elimination
Selective harmonic elimination (SHE) method is basically designed to eliminate undesired low order harmonics through the appropriate choice of the switching angles. Fourier series analysis are normally used to determine the switching angles.

High Switching Frequency Methods
For high power applications, high switching frequency is considered. High switching frequency is employed for with reduced number of voltage levels. Increase in the number of levels at high frequency increases the complexity. High switching frequency methods are attractive for high dynamic range applications due to its improved power quality at higher bandwidth.

Sinusoidal Pulse Width Modulation (SPWM)
The classical SPWM is the very simple and commonly used technique in most of the industrial applications. In the sinusoidal pulse width modulator the gate signals are generated by comparing a three phase balanced sinusoidal reference voltage signal with a high-frequency common triangular carrier voltage signal as shown in the figure 7. The intersection points of these two signals determine the turn on and off time of the switching devices. The amplitude and frequency of the PWM inverter output voltage is determined by considering the sinusoidal reference voltage signal.

Advantages of SPWM
1. Compatible
2. Power consumption is Low.
3. High energy efficient maximum up to 90%.
4. Capability of handling high power.
5. No temperature variation-and ageing-caused, linear degradation.
6. Easy implementation with suitable control techniques.

Disadvantages of SPWM
1. Attenuation of the wanted fundamental component of the waveform
2. Increase in switching frequencies leads to greater stresses on switching devices resulting in de-rating of those devices.
3. Generation of high-frequency harmonic components.

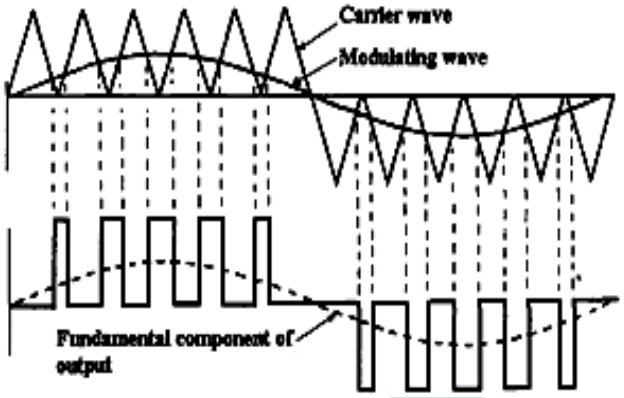

Figure 7: Sinusoidal pulse width modulation

Multicarrier PWM
This method is basically derived from the conventional sinusoidal PWM method. In this method, high frequency multicarrier signals are used and compared with a fundamental frequency sinusoidal reference signal to generate the switching signals for the power switches.
There are two categories of multicarrier PWM that are characterized by the way the carriers are arranged.
Level-shifted PWM- with vertical arrangement of carriers in which each carrier is set in between two voltage levels.
Phase-shifted PWM - arranges the carriers horizontally in which a phase shift is introduced between two carriers.
Level-shifted PWM - suitable for diode-clamped inverter since each carrier signal can be easily related to each power switch.
The reference and carrier signals are continuously compared with each other. When the reference is greater than the carrier, then the power switch associated with this carrier is turned on. If the opposite takes place, then the power switch corresponding to the carrier is turned off. The disposition of the carrier can be divided into three namely:
1. Phase disposition (PD) where all carriers are in phase.
2. Phase opposition disposition (POD) where the carriers above the sinusoidal reference zero point are 180° out of phase with those below the zero point.
3. Alternative phase opposition disposition (APOD) where each carrier is phase shifted by 180° from its adjacent carrier.

Figure 6 shows the classification of modulation techniques. Fundamental switching frequency techniques involve only one of two commutations of power semiconductor switches per cycle of output voltage.

Space Vector Control
Space vector modulation is widely adopted for control of two level VSC whenever the fast dynamic response is necessary. Internally it has a high DC bus voltage utilization

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factor which can be naturally implemented on the hardware circuit. Redundant states are eliminated compared with the other modulation technique.

By sequential switching of power electronic switches the voltage space vector trajectory is obtained where the reference vector is constant. Most commonly used space vector representation in terms of phase voltages are V_{ao},V_{bo},V_{co} on coordinate transformation $T_{\alpha\beta o}$ as

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = T_{\alpha\beta o} \begin{pmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{pmatrix}$$

$$T_{\alpha\beta o} = \begin{pmatrix} 0.5 & 0.5 & \\ 0 & 0.86 & 0.86 \\ 7 & 0.7 & 0.7 \end{pmatrix}$$

Where Tαβo is the transformation on α-β plane.

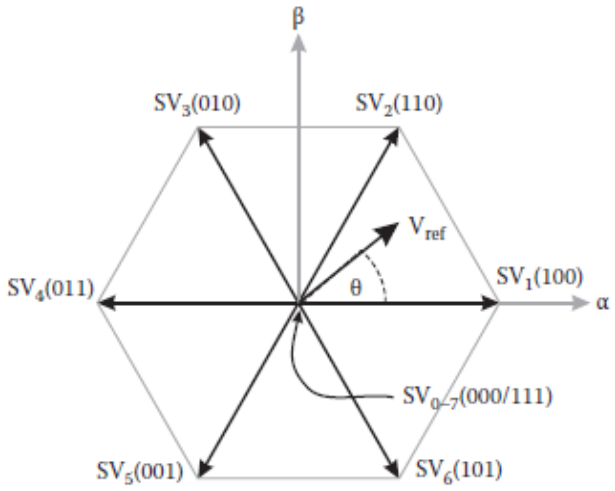

Figure 8: Space vector modulation

Each vector is identified according to *m* for the three phases (*ma mb mc*). Consider a particular case appears for vectors **SV**0 and **SV**7 (zero vectors), where two sets of *ma*, *mb*, and *mc* are the same. **SV**0 is combined connecting the three phases to 0 V i.e when *ma* = *mb* = *mc* = 0, while **SV**7 is obtained with *ma* = *mb* = *mc* = 1. Since both states are equivalent from the point of view of a three-wire load, the selection of the zero vector is commonly used for the reduction of the switching frequency. Switching times are also calculated for each switching state [2].SVPWM principle are feasible for high voltage and high power applications. Space Vector Modulation along with balancing strategy are used to synthesize the desired line voltages at the output maintaining the voltage balance of the DC bus for safe operation of the power devices.

IV. A TECHNICAL LITERATURES SURVEY ON CASCADED MULTILEVEL INVERTER TOPOLOGY AND THE CONTROL TECHNIQUES

Shuvangkar shuvo, eklas hossain, suggested a 5 level and 7 level Symmetric cascaded multilevel inverter. The 5-level inverter proposed has reduced number of switches, cost effective, minimum losses and less complex circuit. Both the inverter are synthesized at 6 KHz switching frequency and the 7 level CHB appears to be the best. An LC filter has been used to reduce THD in the output significantly. Both 5-level and 7-level CHBs have proved almost equal THD levels. Advanced PWM techniques have been investigated to determine their effectiveness in reducing the THD, and providing the best performance [1]. Yidan Li and Bin Wu, discussed about the different topologies and the switching states used by the power switches [2].

Zhong Du, et al., focused on CHM boost inverter for electric vehicle and hybrid Electric Vehicle applications without the use of inductors. Currently existing power inverter systems for hybrid Electric Vehicles uses a dc–dc boost converter to boost the battery voltage compared with traditional three phase inverter [3].

Jianjiang Shi, Wei Gou, Hao Yuan, Tiefu Zhao, proposed solid-state transformer (SST) in power electronic-based microgrid systems where single phase SST consists of a modular multilevel ac–dc rectifier, a modular dual active bridge (DAB) dc–dc converter with high-frequency transformers, and a dc–ac inverter stage. This results in power unbalancing in each module, so hence the modular SST often presents instability problems making its design difficult and causing unpredictable behavior, increase the stress of the semiconductor devices and also cause high harmonic distortions of grid current. To eliminate these problems a novel single-phase d–q vector-based common-duty-ratio control method for the multilevel rectifier and a voltage feedforward, feedback based controller for the modular DAB converter is used [4].

Zhongyuan Cheng, et al. and Bin Wu. , suggested an optimized switching sequences to improve the harmonic and minimizing the switching frequency of a 5-level neutral point clamped H-bridge based inverter on high power multilevel converters applications. The device switching

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frequency is reduced by using a flexible switching pattern. [5].

H. K. Al-Hadidi, et al., suggested the DVRs built using the cascade inverter topology are well suited to compensating sagged voltages at customer loads. For high power factor loads, sag compensation often requires real-power injection using the stored energy on the dc capacitors. Load with low power factors, the compensation can be carried out with zero real power injection for a relatively large sag range. In this paper a thyristor-switched inductor branch during sags is connected intentionally to reduce the power factor. New topology for sag compensation systematically confirmed through electromagnetic transient's simulation and through tests conducted on a prototype DVR [6].

Pablo Lezana, et al., has focused in his literature mainly on the control of 7-level HCMLI with low switching frequency control and how its modulation index can be stretched using triplen harmonic compensation The results established that medium voltage inverter effectively eliminates low frequency input current harmonics at the primary side of the transformer and operates without any problems in regenerative mode [7].

Zhong Du, Leon M. Tolbert, J.-S. Lee, H.-W. Sim, addressed the effects of the connected load to the cascaded H-bridge converter as well as the switching angles on the voltage regulation of the capacitors are studied. This literature proves that voltage regulation is only attainable in a much limited operating conditions that it was originally reported [8-9].

V. MODULATION TECHNIQUES

For multilevel converters there are several methods of modulation techniques that has been developed in the past by the researchers in the power electronics field. Most commonly used techniques are carrier based Sinusoidal PWM and subharmonic elimination modulation techniques. Among the two categories, subharmonic PWM is an elite control approach for multilevel inverters.

1. SINUSOIDAL PWM:

P. Kiruthika, K. Ramani , discussed in detail the principle of different types of multilevel inverter and various control strategies used based on the implementation factor which are most commonly applied[18].

Anaya-Lara, G.M. Burt, D. Telford B.W. Williams J.R. McDonald, suggested the modular multilevel inverter is superior compared with the diode clamped inverter because of several advantages such as phase voltage redundancy, increase in the levels lower will be the THD [19].

Nupur Mittal, Bindeshwar Singh, presented a comparative study on different types and the modulation technique on multilevel inverters focusing mainly on SPWM, SVPWM and SHE-PWM [20].

Abdelaziz Fri, Rachid El Bachtiri, Abdelaziz El Ghzizal presents a comparative study in the Matlab/Simulink environment between Flying Capacitor Multilevel Inverter (FCMLI), the Neutral Point Clamped Multilevel Inverter (NPCMLI), and the Cascaded H-Bridge Multilevel Inverter (H-bridge MLI) based on quality of the output voltage, the complexity and the cost of implementation. Out of these topologies only H-bridge is the most promising topology for PV systems [21].

P.K. Chaturvedi, S. Jain, P. Agarwal, developed a carrier-based closed-loop control technique reducing the switching losses based on insertion of 'no switching' zone within each half cycle of fundamental wave. Efficiency of the inverter system is measured to observe the reduction in switching losses. An improvement of about 5% in efficiency for a switching frequency of 5 kHz is observed with the proposed technique over conventional SPWM technique [22].

Moncef Ben Smida, et al., present a modified topology of stacked multicell converter .Multicarrier subharmonic pulsewidth modulation (PWM), called disposition band carrier and phase-shifted carrier PWM (DBC-PSC-PWM), method is developed to produce (n ×m + 1) output voltage levels and to improve the output voltage harmonic spectrum the control strategy was executed with FPGA of XILINX to control a three-phase SMC 3 × 2 seven-level inverter [23].

K.Ramani, presented a capacitor voltage balancing methods in a flying capacitor multilevel inverter (FCMLI) fed induction motor drive. A seven-level flying capacitor multilevel inverter by using sinusoidal pulse width modulation technique. Based on the pattern the performance in load voltage, total harmonics distortion and capacitor voltage are fluctuated. A 7-L flying capacitor multilevel inverter provides sinusoidal waveform and increased efficiency. A new control scheme has been proposed which uses the preferential charging or discharging of flying the capacitors to balance their voltages. With this control scheme output phase and line voltages are with much less THD. Also used to improve the level of the inverter to extend the design flexibility and reduces the harmonics [24].

2. Selective Harmonic Elimination PWM Technique:

Mahrous Ahmed, Ahmed Sheir, Mohamed Orabi , proposes a genetic algorithm (GA)-based optimization technique to minimize the THD of cascaded H-bridge multilevel inverter.Multilevel inverter have low THD when switching angles are selected at Low frequency. For low-order harmonic minimization, selective harmonic elimination (SHE) is suitable. GA is the finest approach for solving such complex equations by obtaining optimized switching angles.The switching angles are calculated by the genetic algorithm .and applied to a five-level inverter in MATLAB

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Simulink. Cascaded H-bridge configuration is more practically considered than the other two inverter circuit because of less complexity & number of components [25].

Mahrous Ahmed, Ahmed Sheir, proposes a new asymmetric cascaded half H bridge multilevel inverter driven from the conventional asymmetric cascaded half H Bridge multilevel inverter applied for both 7-L and 11-L inverter circuit. With the proper DC sources such as PV or Fuel cells, proposed topology can eliminate the need for polarity generation circuit which normally associated with the cascaded half H-bridge. Which results in simplicity, modularity in control and construction along with reduces number of switches that require high blocking voltage. Selective harmonic elimination SHE method is applied to generate switching pattern to eliminate harmonics inherently associated with MLI. By reducing the voltage stress, switching losses and finally decrease in the size and cost [26].

T.jeevabharathi, v.padmathilagam, the author has proposed Particle Swarm Optimization approach along with the SHE problem with unequal dc sources. The number of switching angles is increased and the determination of these angles using conventional iterative methods as well as the resultant theory is impossible. The proposed approach also reduces the computational burden to find the optimal solution compared with conventional iterative methods. The elimination of harmonics in an 11-Level Cascaded Multilevel Inverter (CMLI) by considering the separate unequal dc sources by using Particle Swarm Optimization (PSO) is analyzed. This analysis effectively eliminates the number of specific harmonics, and the output voltage is resulted in low total harmonic distortion [27].

Sridhar R. Pulikanti, et al., proposed a 5-Level flying-capacitor based active-neutral-point-clamped converter. To regulate the voltage in FCs a control strategy by swapping the switching patterns of power switches based on the polarity of the current , the polarity of the voltage, and the polarity of the fundamental line-to-neutral voltage under selective harmonic elimination pulse width modulation. The voltage across the FCs and the dc-link capacitors are simultaneously controlled at their reference voltage levels. This control strategy is applied using power system computer aided design including dc on a static synchronous compensator operating under a power-factor-correction mode to evaluate its performance [28].

Sridhar R. Pulikanti, Mohamed S. A. Dahidah, proposes a control strategy for neutral point voltage balancing based on SHE-PWM suitable for three-level ANPC converters. A small change in the switching angles, varies the duty cycle of the zero-level switching state, controls the neutral point current and therefore the neutral point voltage. Considering the output currents and the voltage across the lower dc-link capacitor. An optimized SHE-PWM approaches is considered from the fact that the harmonic spectrum is tightly controlled by minimizing harmonic filter requirements and eliminating expensive and large reactive components. Furthermore, it provides the ability for natural balancing of the neutral point voltage due to symmetrical pulse patterns. Switching transitions per fundamental cycle decreases in SHE-PWM when compared to the conventional carrier-based PWM techniques for the same bandwidth and hence associated converter switching losses will also decrease .With the dynamic approach that deals with voltage ripple across dc-link capacitors by varying SHE-PWM switching angles based on the capacitance of the dc-link capacitors and the operating point in a STATCOM application was also discussed in detail [29].

H. Taghizadeh, et al., proposes an idea to eliminate the harmonics in a cascade multilevel inverter by considering the separate unequal dc sources by using particle swarm optimization [30].

Fanghua Zhang, et al., proposed a three-phase four-leg inverter with selective harmonic elimination (SHE).The control signals of the four legs are calculated and analyzed in such a way to eliminates lower order non-triplen harmonics. The ratio of switching-to-fundamental frequency is only 13 and 27 (per unit) p.u. for the three legs and the fourth leg with the total harmonic distortion of output voltage lower than 4%. Along with the ability to carry unbalanced loads. This is also used in high-power, medium- or high-fundamental-frequency applications [31].

VI. ANALYSIS OF THE PROPOSED PAPER

From Table 2 given below, summarizes that about 22.58 % of total review literature are based on Sinusoidal PWM Technique and 25.80% based on the Selective Harmonic Elimination PWM Technique.

Table-2: Literature Review Papers on Modulation Techniques

Parameters	Total No. of Literatures Reviews out of 31 Literatures	% of Literature Review in Modulation Technique
SPWM	07	22.58
SHE-PWM	08	25.80

VII. CONCLUSIONS

This paper gives us an insight about the various technical literatures concerned with Cascaded Multilevel Inverter along with their merits and demerits based on the inherent characteristics of the SPWM and SHE modulation techniques. These modulation techniques are commonly used for both medium and high power applications. The main advantage of MLI family is that it finds a solution to

the problems of total harmonics distortion, EMI, and dv/dt stress on switch. This paper focuses on the fundamental principles of cascaded multilevel inverters. The survey carried out will be helpful for the researchers for finding out the relevant references as well as comparing with the previous work which is carried out in the field of cascaded multilevel inverter topologies and their modulation technique.

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