ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

Analysis of fuzzy logic controller based dual voltage source inverter to compensate unbalanced and nonlinear loads

[1]M. Sreelekha, [2] K. Ravi Sankar M.Tech,(Ph.D)
[1] pg scholar [2] Academic Assistant professor.
[1][2] Department of EEE JNTUA College of Engineering Pulivendula, Andhra Pradesh.

Abstract— This paper describes Fuzzy logic controller dual voltage source inverter (DVSI) to enhance the reliability and power quality of microgrid system. The reference currents for this scheme are produced by using ISCT (Instantaneous symmetrical component theory).ISCT makes DVSI to operate in grid injecting and grid sharing modes. This scheme makes the microgrid to exchange power generated by Distribution Energy Resources (DERs) and also to compensate the local unbalanced nonlinear loads. Fuzzy logic controller (FLC) is used in this proposed scheme instead of PI controller for the better quality of power. This proposed system topology is modeled and simulated in MATLAB/SIMULINK environment.

Index Terms—. Fuzzy logic controller (FLC), Grid connected inverter, Instantaneous symmetrical component theory (ISCT)., microgrid,powerquality

I. INTRODUCTION

The propagation of power electronic devices and electrical loads with unbalanced and nonlinear currents has degraded the power quality in the power distribution network. Moreover, the voltage at the point of common coupling (PCC) is distorted by the harmonic currents if there is a considerable amount of feeder impedance in the distribution systems [1]. Existing method describes the single inverter system with multi functional capabilities that is it would facilitates the active power injection from a local distribution energy resources(DERs) like solar photo voltaic (PV) system and also operates as an active power filter [2]. In the case of high insolation periods, huge amount of reactive power is required to adjust the voltage at the (PCC).But with the supply of active and reactive power by only one single inverter either real power injection or load compensation capabilities may degraded [3]. This paper describes a DVSI scheme, in which the power generated by the DERs is supplied as real power by the main voltage source inverter (MVSI) and the reactive, unbalanced and harmonic load compensation is supported by auxiliary voltage source inverter (AVSI).This proposed DVSI method will increase the reliability and makes the better utilization of power produced by distributed energy source.

II. PROPOSED DVSI METHOD:

A. System Topology:

The proposed DVSI topology is shown in fig1.As shown in fig1; Neutral point clamped (NPC) inverter works as AVSI and three-leg inverter works as the MVSI [4]. These MVSI and AVSIs are connected at the PCC and these are supplying the nonlinear and unbalanced load. AVSI compensates the unbalanced, reactive and harmonic components in the load currents.i_{la}, i_{lb} , i_{lc} are load currents in the three phases. $i_{g(abc)}$ denotes grid currents in the three phases and $i_{\mu gx(abc)}$, $i_{\mu gm(abc)}$ denotes AVSI and MVSI currents in the three phases respectively. At the dc link of AVSI, Split capacitor topology is used with capacitors C1 and C2.

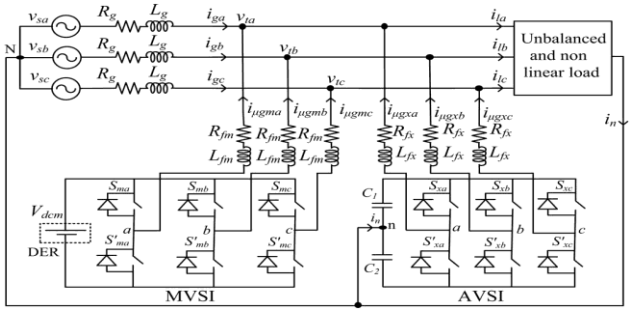

Fig.1. proposed Topology of DVSI scheme.

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

The Power which is available at the DERs is supplied by the MVSI. Distributed energy source is represented as the DC voltage source in the fig1. MVSI and AVSI are connected at PCC through interfacing inductance. Interfacing inductance value needed for AVSI is more compared to interfacing inductance value needed by MVSI. AVSI supplies unbalanced nonlinear currents but MVSI supplies balanced and sinusoidal currents. Because of switching operation of power electronic IGBT switches high frequency components may be generated. Interfacing inductances will eliminate these high switching frequency components.

B. Designing of DVSI parameters:

1) AVSI: Designing method of split capacitor DSTATCOM topology has been utilized for the AVSI parameters like hysteresis band($\pm h_x$),dc storage capacitors(C_1,C_2), dc link voltage (V_{dc}) , interfacing inductance(L_{fx})[5].The dc-link voltage across each capacitor is taken as 1.6 times the peak of phase voltage and total dc-link voltage reference (V_{ref}) is found to be 1040v.Based on the changing of V_{dc} in the transient periods the dc capacitor values of DVSI are chosen. Let total rating of the load is SKVA. In the worst case, the load power may fluctuate from 0 to SKVA. To maintain the load power demand during transients the exchanging of real power is needed by the AVSI. Capacitor voltage deviation from its reference value may occur during transients due to transfer of real power. Assume that the voltage controller takes n cycles, i.e., nT seconds to act, where T is the system time period. Hence, during transients the maximum power exchange by AVSI will be nST. This energy will be equal to change in the capacitor stored energy. Therefore

$$\frac{1}{2} C_1 (V^2_{dcr}-V^2_{dc1}) = nST \qquad \text{---------- (1)}$$

Where V_{dcr} is dc reference voltage and V_{dc1} is maximum permissible dc-link voltage across capacitor C_1 during transient.Here,S=5KVA,V_{dcr}=520V,V_{dc1}=0.8*V_{dcr} or1.2*V_{dcr}, n=1 and T=0.02 s. By substituting above values in(1),the dc-link capacitance (C_1) is calculated to be 2000μF. Same value of capacitor is chosen for C_2.The interfacing inductance is given as follows

$$L_{fx} = \frac{1.6Vm}{4hxfmax} \qquad \text{---------- (2)}$$

Assuming maximum switching frequency (f_{max}) as of 10 KHZ and hysteresis band (h_x) as 5% of load current (0.5A), then the value of L_{fx} is obtained is 26mH.

2) MVSI: The MVSI uses a three-leg inverter topology. Dc-link voltage of MVSI is obtained as 1.15*V_{ml}, where V_{ml} is the peak value of line voltage. This value of this obtained is 648V. Balanced sinusoidal current at unity power factor is supplied by MVSI. So the output current of MVSI doesn't contain zero sequence switching harmonics. This makes the requirement of filter less for MVSI as compared to AVSI [6]. In this analysis, a filter inductance (L_{fm}) of 5mH is used.

III. DVSI SCHEME CONTROL STRATEGY:

A. Fundamental voltage extraction: PCC voltages may be distorted because of the presence of feeder impedance in the system. Therefore, for the reference current generation the fundamental positive sequence components of the PCC voltages are extracted. To convert the distorted PCC voltages to balanced sinusoidal voltages dq0 transformation is used. The PCC voltages in natural reference frame (v_{ta}, v_{tb} and v_{tc}) are first transformed into dq0 reference frame as follows,

$$\begin{bmatrix} Vtd \\ Vtq \\ Vt0 \end{bmatrix} = C \begin{bmatrix} Vta \\ Vtb \\ Vtc \end{bmatrix} \qquad \text{---------- (3)}$$

Where

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

Modified synchronous reference frame (SRF) phase locked loop (PLL) is used to get θ [7]. The schematic diagram of this PLL shown in fig2.In this PLL, the SRF terminal voltage in q-axis (V_{tq}) is

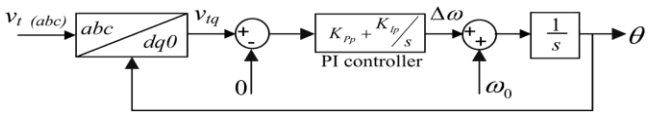

Fig2 : schematic diagram of PLL

Compared with 0V and the error voltage thus obtained is given to the PI controller. The frequency deviation Δw is then added to the reference frequency w_0 and finally given to the integrator to get θ. As PCC voltages are distorted, the transformed voltages in dq0 frame (v_{td} and v_{tq}) contain average and oscillating components of voltages. These can be represented as

$$V_{td} = \bar{V}_{td} + \tilde{V}_{td} \quad , \quad V_{tq} = \bar{V}_{tq} + \tilde{V}_{tq} \quad \text{----------(4)}$$

Where $\bar{V}_{td}$, $\bar{V}_{tq}$ represent the average components and $\tilde{V}_{td}$, $\tilde{V}_{tq}$ represents oscillating components of V_{td} and V_{tq} respectively. Now the fundamental positive sequence of PCC voltages in natural reference frame can be obtained with the help of inverse dq0 transformation.

$$\begin{bmatrix} V_{ta1}^{+} \\ V_{tb1}^{+} \\ V_{tc1}^{+} \end{bmatrix} = C^{T} \begin{bmatrix} \bar{V}td \\ \bar{V}tq \\ 0 \end{bmatrix} \quad \text{---------- (5)}$$

These voltages $V_{ta1}^{+}, V_{tb1}^{+}, V_{tc1}^{+}$ are used in the reference current generation algorithms, so as to draw balanced sinusoidal currents from the grid.

B. Instantaneous symmetrical component Theory: The schematic of system used for realizing the reference current for the compensator is shown in below figure3 [8].

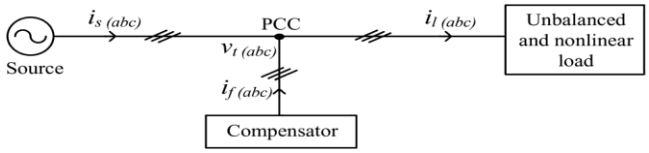

Fig3: Schematic of an unbalanced and non linear load compensation scheme.

The ISCT for load compensation is derived based on the following three conditions.

1) The source neutral current must be zero. Therefore

$$i_{sa} + i_{sb} + i_{sc} = 0 \quad \text{----------(6)}$$

2) The phase angle between the fundamental positive sequence voltage (V_{ta1}^{+}) and source current (i_{sa}) is $\emptyset$

$$\angle V_{ta1}^{+} = \angle i_{sa} + \emptyset \quad \text{--------- (7)}$$

3) The average real power of the load (p_l) should be supplied by the source

$$V_{ta1}^{+} i_{sa} + V_{tb1}^{+} i_{sb} + V_{tc1}^{+} i_{sc} = p_l \quad \text{----------(8)}$$

Solving the above three equations, the reference source currents can be obtained as

$$i_{sa}^{*} = \left(\frac{V_{ta1}^{+} + \beta (V_{tb1}^{+} - V_{tc1}^{+})}{\Sigma_{j=a,b,c} V_{tj}^{+2}} \right) p_l$$

$$i_{sb}^{*} = \left(\frac{V_{tb1}^{+} + \beta (V_{tc1}^{+} - V_{ta1}^{+})}{\Sigma_{j=a,b,c} V_{tj}^{+2}} \right) p_l \quad \text{--------(9)}$$

$$i_{sc}^{*} = \left(\frac{V_{tc1}^{+} + \beta (V_{ta1}^{+} - V_{tb1}^{+})}{\Sigma_{j=a,b,c} V_{tj}^{+2}} \right) p_l$$

Where $\beta = \frac{\tan \emptyset}{\sqrt{3}}$.The term $\emptyset$ is desired phase angle between the fundamental positive sequence of PCC voltage and source current. To get unity power factor for source current, substitute β=0 in equation (9). Thus the reference source currents for three phases are given by

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

$$i^*_{s(abc)} = \left(\frac{V_{t(abc)1}{}^{+})}{\Sigma_{j=a,b,c} V_{tj}{}^{+2}} \right) p_l \qquad \text{----------(10)}$$

Where i^*_{sa}, i^*_{sb}, i^*_{sc} are fundamental positive sequence of load currents drawn from the source, when it is supplying an average load power p_l. The power P_l can be computed using a moving average filter with a window of one-cycle data points as given below

$$P_l = \frac{1}{T} \int_{t1-T}^{t1} (V_{ta1}{}^{+} i_{la} + V_{tb1}{}^{+} i_{lb} + V_{tc1}{}^{+} i_{lc}) dt \text{ ----- (11)}$$

Where t_1 is any arbitrary time instant. Finally, the reference currents for the compensator can be generated as follows:

$$i^*_{f(abc)} = i_{l(abc)} - i^*_{s(abc)} \qquad \text{----------(12)}$$

Equation (12) can be used to generate the reference filter currents using ISCT, when the entire load active power, P_l is supplied by source and load compensation is performed by a single inverter. The source currents, $i_{s(abc)}$ and filter currents $i_{f(abc)}$ will be equivalently represented as grid currents $i_{g(abc)}$ and AVSI currents $i\mu gx(abc)$, respectively.

C. Control strategy of DVSI: Control strategy of DVSI is developed in such a way that grid and MVSI together share the active load power, and AVSI supplies rest of the power components demanded by the load.

1) Reference current generation for AVSI:

The dc-link voltage of the AVSI should be maintained constant for proper functioning of the auxiliary inverter. DC-link voltage variation occurs in auxiliary inverter due to its switching and ohmic losses. These losses expressed as P_{loss} must be supplied by the grid. An expression for p_{loss} is derived on the condition that average dc capacitor current is zero to maintain a constant capacitor voltage [8]. The deviation of average capacitor current from zero will reflect as a change in capacitor voltage from a steady state value. A PI controller is used to produce p_{loss} term as given by

$$P_{loss} = K_{pv} e_{vdc} + K_{Iv} \int e_{vdc} dt \qquad \text{---------- (13)}$$

Where $e_{vdc}=V_{dcerf} - v_{dc}$, v_{dc} represents the actual voltage sensed and updated once in a cycle. In the above equation, K_{pv} and K_{Iv} represent the proportional gain and integral gains of dc-link PI controller, respectively.

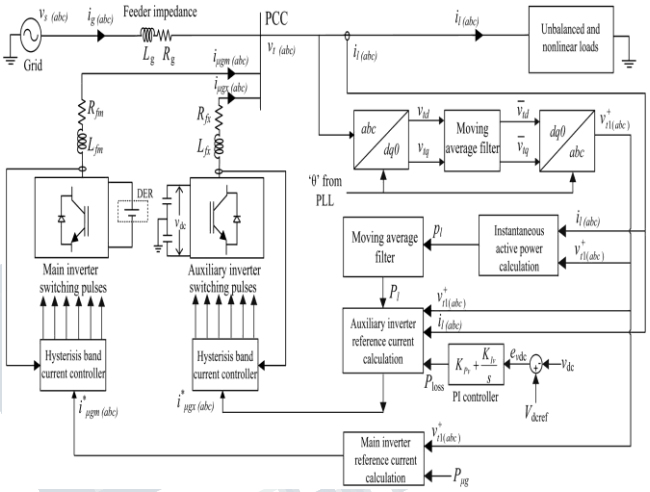

Fig: 4 Schematic diagram showing the control strategy of proposed DVSI scheme

AVSI reference currents are obtained as given in equation (14). Here, the dc-link voltage PI controller gains are selected so as to ensure stability and better dynamic response during load change [9].

$$i^*_{\mu gxa} = i_{la} - \left(\frac{V_{ta1}{}^{+}}{\Sigma_{j=a,b,c} V_{tj}{}^{+2}} \right) (p_l + p_{loss})$$

$$i^*_{\mu gxb} = i_{lb} - \left(\frac{V_{tb1}{}^{+}}{\Sigma_{j=a,b,c} V_{tj}{}^{+2}} \right) (p_l + p_{loss}) \qquad \text{--------(14)}$$

$$i^*_{\mu gxc} = i_{lc} - \left(\frac{V_{tc1}{}^{+}}{\Sigma_{j=a,b,c} V_{tj}{}^{+2}} \right) (p_l + p_{loss})$$

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

2) Reference current generation for MVSI:

MVSI supplies balanced sinusoidal currents based on the produced power at DER. If MVSI losses are neglected, the power injected to grid will be equal to that available at DER ($p_{\mu g}$). The following equation, which is derived from ISCT can be used to generate MVSI reference currents for three phases (a, b, and c)

$$i^*_{\mu gm(abc)} = \left(\frac{V_{t(abc)1}{}^+}{\Sigma_{j=a,b,c} V_{tj}{}^{+2}}\right) p_{\mu g} \text{ --------- (15)}$$

Where $p_{\mu g}$ is the available power at the dc link of MVSI. The reference currents obtained from (14) to (15) are tracked by using hysteresis band current controller (HBCC). HBCC schemes are based on a feedback loop. Applying Kirchhoff's current law (KCL) at the PCC in Fig.4

$$i_{\mu gxj} = i_{lj} - (i_{gj} + i_{\mu gmj}), \text{ for j=a, b, c -------- (16)}$$

By using (14) and (16), an expression for reference grid current in phase-a (i^*_{ga}) can be obtained as

$$i^*_{ga} = \left(\frac{V_{ta1}{}^+}{\Sigma_{j=a,b,c} V_{tj}{}^{+2}}\right) [(p_l + p_{loss}) - p_{\mu g}] \text{ --------- (17)}$$

It can be observed that, if the quantity (p_l+p_{loss}) is greater then $p_{\mu g}$, the term[(p_l+p_{loss})- $p_{\mu g}$] will be a positive quantity, and i^*_{ga} will be in phase with v^+_{ta1}.This operation can be called as the grid supporting or grid sharing mode, as the total load power demand is shared between the main inverter and the grid. The term, p_{loss} is usually very small compared to p_l. on the other hand, if (p_l + p_{loss}) is less than $p_{\mu g}$, then [(p_l+p_{loss})- $p_{\mu g}$] will be a negative quantity, and hence i^*_{ga} will be in phase opposition with v^+_{ta1}. This mode of operation is called the grid injecting mode, as the excess power is injected to grid.

IV. FUZZY LOGIC CONTROLLER:

To maintain the dc-link voltage constant Fuzzy logic controller is used in this project. error in dc-link voltage and change in dc-link voltages are the two inputs for the Fuzzy logic controller in this project. Total harmonic distortion values in the system are decreased by using Fuzzy controller instead of using PI controller. The steps involved in the whole process are Fuzzification, Inference method and Defuzzification.

$e/\Delta e$	NE	ZE	PE
NCE	N	N	N
ZCE	N	Z	P
PCE	P	P	P

Table 1: Fuzzy Rules Set

The above Table shows the different relations between the two inputs of the FLC and the output. This table is called the Rule Base of the FLC. Here NE,ZE,PE are negative, zero, positive errors respectively and NCE,ZCE,PCE are negative, zero, positive change in errors respectively and N,P,Z are negative, positive, zero representations in output. e,Δe are error and change in errors respectively. The interference method used is the Mamdani method. The defuzzification method used is the Centroid method.

V. SIMULATION RESULTS:

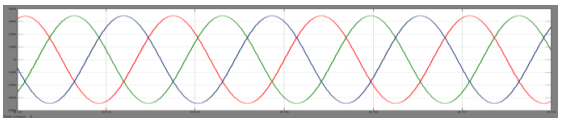

Fig5: Without DVSI scheme: (a) PCC voltages

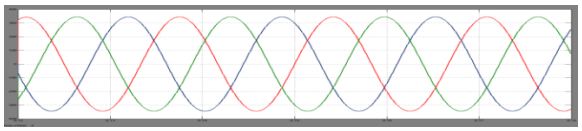

Fig6: Without DVSI scheme (b) Fundamental positive sequence of PCC voltages

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

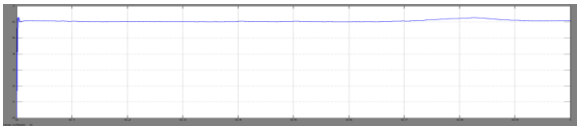

Fig7. Active power sharing: (a) load active power

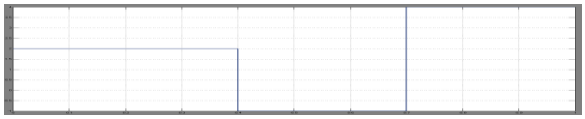

Fig8. Active power sharing: (b) active power supplied by grid

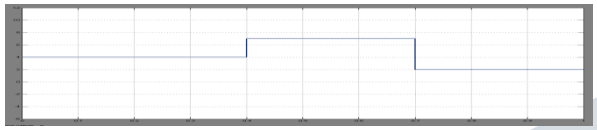

Fig9. Active power sharing: (c) active power supplied by MVSI

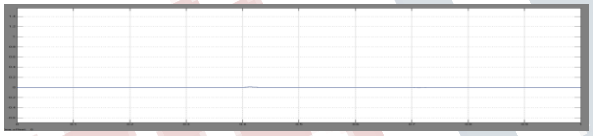

Fig10. Active power sharing: (d) active power supplied by AVSI

Fig11. Reactive power sharing: (a) load reactive power

Fig12. Reactive power sharing: (b) reactive power supplied by AVSI

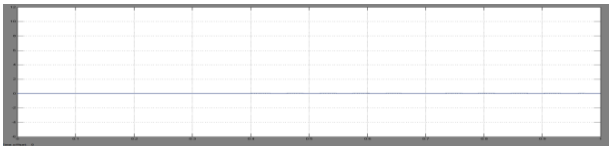

Fig.13. Reactive power sharing: (c) reactive power supplied by MVSI

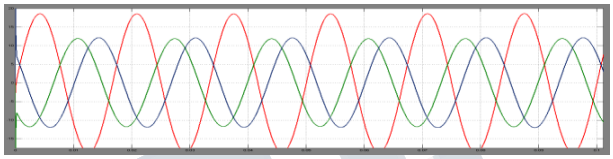

Fig.14. Simulated performance of DVSI scheme: (a) load currents

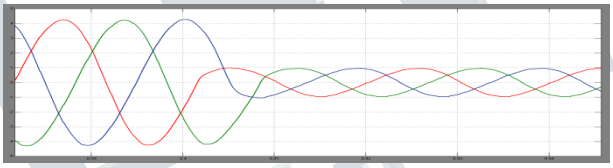

Fig.15. Simulated performance of DVSI scheme: (b) grid currents

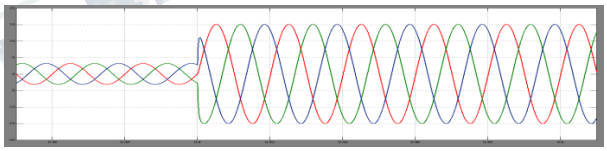

Fig.16. Simulated performance of DVSI scheme: (c) MVSI currents

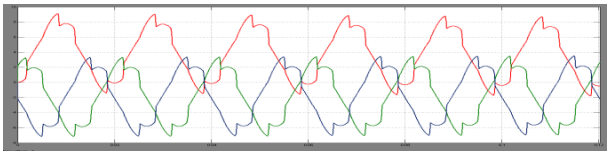

Fig.17. Simulated performance of DVSI scheme: (d) AVSI currents

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

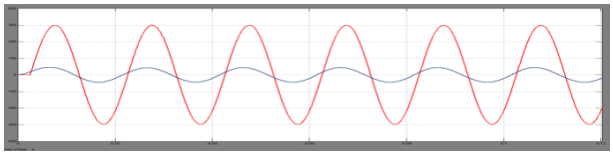

Fig.18. Grid sharing and grid injecting modes of operation: (a) PCC voltage and grid current (phase-a)

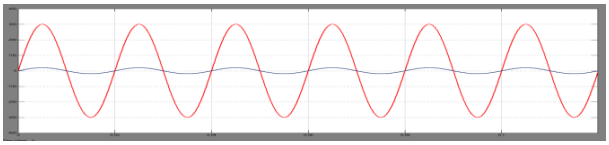

Fig.19. Grid sharing and grid injecting modes of operation: (b) PCC voltage and MVSI current (phase-a).

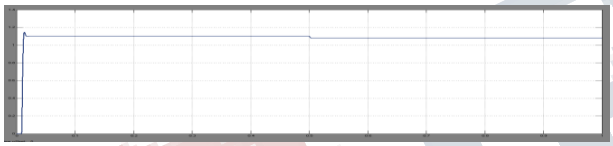

Fig.20. DC-link voltage of AVSI

VI. FFT ANALYSIS:

FFT Analysis is done for different waveforms by using PI controller and Fuzzy logic controller in the system is as given below. Total Harmonic Distortion (THD) is decreased by using the Fuzzy Logic controller as compared to PI controller.

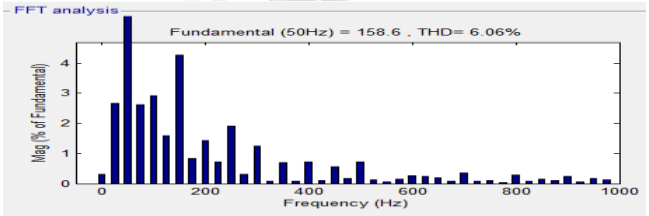

Fig:21(a) Harmonis spectrum of Grid Voltage with PI controller in the system

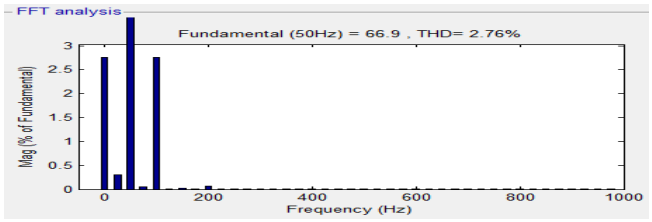

Fig: 21(b): Harmonic spectrum of Grid Voltage with Fuzzy Logic Controller in the system

VII. THD COMPARISON WITH PI AND FUZZY LOGIC CONTROLLERS:

%THD comparison with PI and Fuzzy controllers is mentioned in below table. From this table we can observe that by using Fuzzy controller instead of PI controller the Total Harmonic Distortion value decreased and Power quality has improved.

Waveform	%THD with PI controller	%THD with Fuzzy controller
Grid voltage	6.06	2.76
Grid current	2.71	1.36
Load current	43.47	22.55
Load voltage	1.40	0.24
MVSI current	0.32	0.03
AVSI current	14.03	13.96

Table 2: %THD comparison of waveforms with PI and fuzzy controllers.

VIII. CONCLUSION:

In this paper we have explored the grid connected dual voltage source inverter with fuzzy logic controller to exchange the power generated by Distributed Generators (DGs) with Grid and also to compensate the local unbalanced and nonlinear load. As compared to a single inverter with multifunctional capabilities, a DVSI has many advantages such as, more utilization of inverter capacity to inject real power from DGs to microgrid and as separate dc-link are provided for both inverters the reliability of system increases because if one of those two inverters may get failed, in that case another will operate uninterruptedly.

ISSN (Online) 2395-2717

International Journal of Engineering Research in Electrical and Electronic Engineering (IJEREEE)
Vol 3, Issue 9, September 2017

REFERENCES:

[1] R. Majumder, A. Ghosh, G. Ledwich, and F. Zare, "Load sharing and power quality enhanced operation of a distributed microgrid," *IET Renewable Power Gener.*, vol. 3, no. 2, pp. 109–119, Jun. 2009

[2] M. Schonardie, R. Coelho, R. Schweitzer, and D. Martins, "Control of the active and reactive power using dq0 transformation in a three-phase grid-connected PV system," in *Proc. IEEE Int. Symp. Ind. Electron.*, May 2012, pp. 264–269.

[3] R. Tonkoski, D. Turcotte, and T. H. M. EL-Fouly, "Impact of high PV penetration on voltage profiles in residential neighborhoods," *IEEE Trans. Sustain. Energy*, vol. 3, no. 3, pp. 518–527, Jul. 2012

[4] S. Iyer, A. Ghosh, and A. Joshi, "Inverter topologies for DSTATCOM applications—A simulation study," *Electr. Power Syst. Res.*, vol. 75, no. 23, pp. 161–170, 2005.

[5] U. Rao, M. K. Mishra, and A. Ghosh, "Control strategies for load compensation using instantaneous symmetrical component theory under different supply voltages," *IEEE Trans. Power Del.*, vol. 23, no. 4, pp. 2310–2317, Oct. 2008.

[6] M. Prodanovic and T. Green, "Control and filter design of three-phase inverters for high power quality grid connection," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 373–380, Jan. 2003.

[7] L. Rolim, D. da Costa, and M. Aredes, "Analysis and software imple- mentation of a robust synchronizing PLL circuit based on the pq theory," *IEEE Trans. Ind. Electron.*, vol. 53, no. 6, pp. 1919–1926, Dec. 2006.

[8] A. Ghosh and A. Joshi, "A new approach to load balancing and power factor correction in power distribution system," *IEEE Trans. Power Del.*, vol. 15, no. 1, pp. 417–422, Jan. 2000.

[9] L. Shiguo, "Optimal design of dc voltage close loop control for an active power filter," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, Feb. 1995, pp. 565–570.