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Design of Schmitt-Trigger-Based Low Power 12T SRAM cell

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Abstract-— **As the technology is being scaled down leakage power is becoming an important contributing factor in total power dissipation of the circuit. So in the portable electronic devices such as cell phones, laptops emphasis has to be given to reduce power consumption during active as well as standby mode. This paper presents a Schmitt-trigger-based 12T SRAM cell which consumes lowest average power as well as lowest leakage power among the cells considered for comparison. The results have been obtained using Cadence Virtuoso Tool with 180nm Technology. The layout is drawn in 180nm technology to layout versus schematic for the proposed 12T SRAM cell.**

I. INTRODUCTION:

Portable electronic devices have extremely low power requirement to maximize the battery lifetime. Various device/circuit/architectural level techniques have been implemented to minimize the power consumption. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the threshold voltage of the device will also get reduced. According to leakage current equation, leakage current has an inverse relationship with the threshold voltage, hence the threshold voltage has to be increased to reduce the leakage power. However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for SRAM bitcells using minimum-sized transistors.

SRAM makes up a large portion of a system-on-chip area, and most of the time, it also dominates the overall performance of a system. In addition to this, the tremendous growth in the popularity of mobile devices and other emerging applications, such as implanted medical instruments and wireless body sensing networks, necessitates the requirement of low-power SRAMs. Therefore, a robust low-power SRAM circuit design has drawn great research attention and has become important. However, a design of robust low-power SRAM faces many process and performance related challenges. This is because, in deep submicrometer technology, near/subthreshold operation is very challenging due to increased device variations and reduced design margins. In addition, with each technology node, the share of leakage power in the total power dissipated by a circuit is increasing. Since, most of the time, SRAM cells stay in the standby mode, thus, leakage power is very important.

II. SINGLE ENDED SRAM TOPOLOGIES

Single-ended SRAM topology is one of the very useful approaches for power-constrained applications. It reduces the leakage and switching power and also saves chip area. BLs have very high capacitance loading, particularly for sub-100- nm regime. During each read/write operation, the switching of BL costs significant dynamic power consumption. The single-ended scheme reduces one half of the active power for BL switching. However, it incurs penalty in terms of increased read/write access time and degraded write 1 SNM at low supply voltages. This is the major limitation of a single-ended SRAM structure.

III. PROPOSED ST BASED12T SRAM CELL DESIGN

A.SCHMITT TRIGGER INVERTER

The stability of cross-coupled inverter pair in SRAM cell operating at very low supply voltage is not very promising. Furthermore, power consumption is high due to degraded inverter characteristic. Therefore, a Schmitt Trigger inverter (ST inverter) is used to exploit the improved inverter characteristic. The basic element for the data storage in an ST-based SRAM cell uses a cross-coupled ST-based inverter pair shown in Fig. 1(a). ST is like a comparator, which includes positive feedback. Considering the switching of output voltage, V_{out} from 1 to 0, in the case of inverter, the transition starts as soon as the input voltage reaches the threshold voltage of the PD transistor, Vthn. On the other hand, in case of ST-based inverter, for Vout = 1, the feedback

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transistor MNF is ON and the voltage at node VNX is Vdd − Vthn. In this case, the minimum voltage required at the input for switching will be much higher than Vthn. The characteristic for inverter and ST is shown in Fig. 1(b). Due to the improved inverter characteristic, the ST-based SRAM offers higher SNM much higher than Vthn. The characteristic for inverter and ST is shown in Fig. 1(b). Due to the improved inverter characteristic, the ST-based SRAM offers higher SNM.

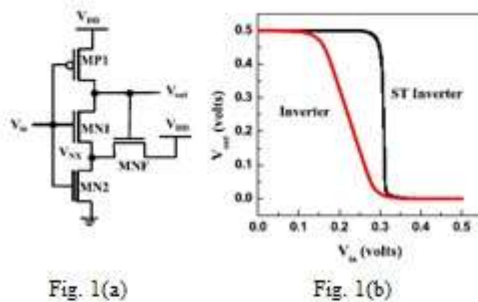

Fig. 1(a) Basic ST Inverter (b) Characteristics of ST Inverter for 0 to 1 transition at the input.

B.PREVIOUS ST11T SRAM CELL APPROACH

The schematic of ST 11T SRAM cell is shown in Fig. 3.1. The ST11T SRAM Cell consists of a cell core (cross-coupled ST inverter), a read path consisting of two transistors, and a write-access transistor. The write-access transistor M9 is controlled by row-based WL, and the read-access transistor M10 is controlled by row-based read WL (RWL). The feedback transistors of ST, M7 and M8 are controlled by internal storage nodes Q and QB, respectively, with their drains connected with a control signal Wordline_bar (WLB) (inverted version of write enable signal).

In the hold mode, both WL and RWL are disabled. Therefore, the cross-coupled ST inverter is isolated from both the BLs, and the data-holding capability is increased due to the feedback mechanism.

During read operation, WL is disabled, whereas RWL is enabled, which provides discharging path for RBL through transistors M10 and M11 depending on the data stored at QB. The disabled WL makes data storage nodes (Q and QB) decoupled from BL during the read access. Due to this isolation, the RSNM is almost the same as the HSNM. Since the HSNM is very high in ST- based cell, read stability is remarkably improved. It is to be noted that in both read and hold mode, WLB is at Vdd (because write enable signal is disabled), which helps the feedback transistors M7 and M8 to provide a feedback mechanism and to exploit the feature of ST inverter to have a good inverter characteristic.

For writing data into the cell, WL is activated to transfer the data to storage node from BL, which is set/reset according to the data to be written. RWL is disabled. The WLB signal, which is inverted version of write enable signal, is disabled (i.e., WLB = 0 V) during the write operation. Consequently, there is no feedback action from any of the feedback transistors M7 and M8 as the voltage at nodes NL and NR does not rise.

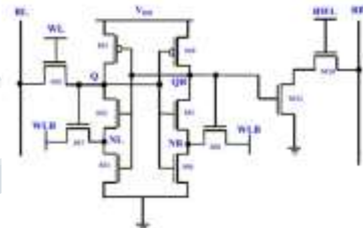

Fig. 3.1 ST 11T SRAM Cell

C.PROPOSED ST 12T SRAM CELL

The Schematic of ST 12T SRAM Cell is as shown in Fig. 3.2

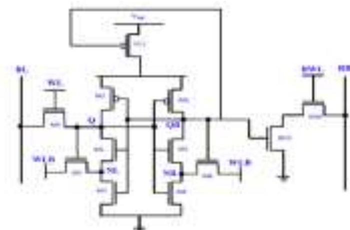

Fig. 3.2 ST 12T SRAM CELL

During hold mode WL and RWL are disabled, hence the cross coupled inverter is isolated from both the bit lines. We can't perform either read or write operation during hold mode.

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During read operation, WL is disabled, but RWL is enabled and RBL is enabled, so that the data present in the storage node Q can be accessed at the drain terminal of MAR2.

During write operation, WL is enabled, but RWL is disabled, so that a new data can be written in to the data storage node Q through a bit line BL.

The transistor M12 is used as a conditional pull up control which helps to reduce further power consumption compared to ST 11T SRAM cell

IV. CELL PERFORMANCE AND COMPARISON

A. Read/write Power

In this Paper Read/write power Comparison of the proposed design is carried out with various SRAM Cells like 6T, 7T, 8T, 10T, and
11T SRAM cells. Simulation Results Shows That the Proposed 12T SRAM Cell Consumes less read/write power.

B. Leakage power

At deep submicrometer technology nodes, the subthreshold leakage in embedded cache becomes a serious issue. It is the cross-coupled inverter that mainly contributes to leakage power of an SRAM cell. For the proposed cell, there is stacking of transistors during both hold 0 and hold 1 state. In addition, the devices in the cross- coupled ST inverter are of a minimum size. Consequently, the combined effect of stacking and minimum sizing leads to a very low leakage power in the ST12T cell.

The schematics of other SRAM Cells considered for power comparison are given below.

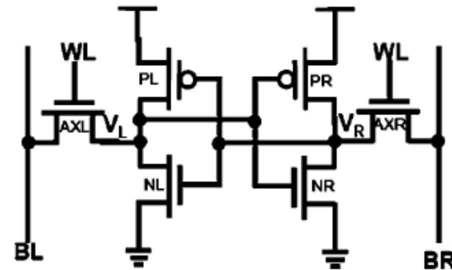

Fig. 4.1 Differential 6T SRAM Cell

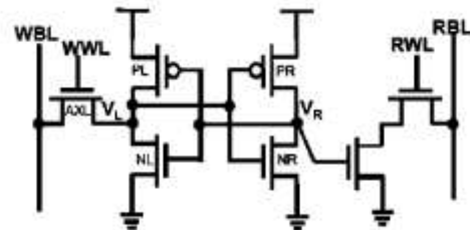

Fig. 4.2 Single ended 7T SRAM cell

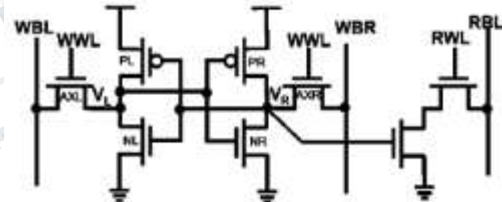

Fig. 4.3 Single ended 8T SRAM cell

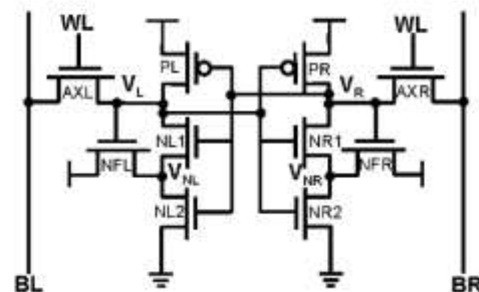

Fig. 4.4 Differential 10T SRAM cell

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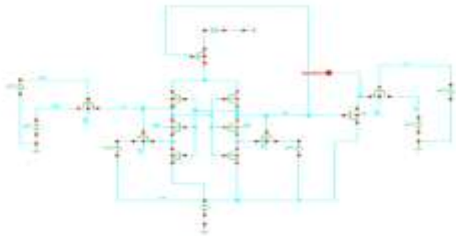
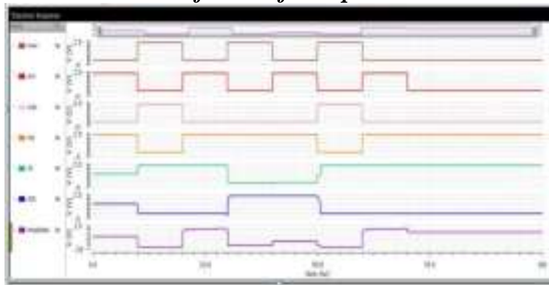
V. SIMULATION RESULTS

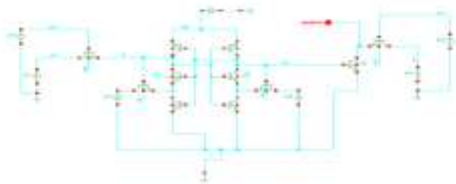
A. Proposed 12T SRAM cell Schematic.



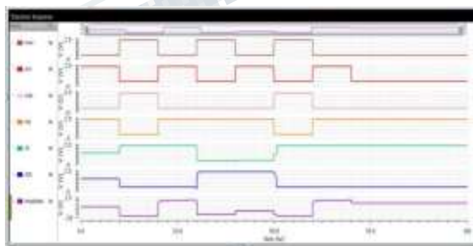
B. Read/Write Waveforms of Proposed 12T SRAM cell



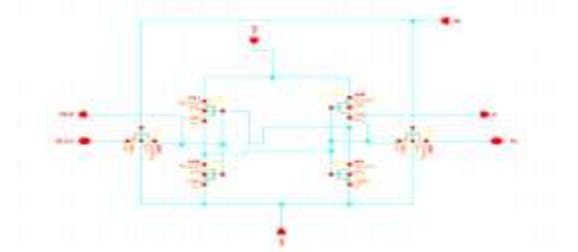
C. Schmitt Trigger Based 11T SRAM cell Schematic



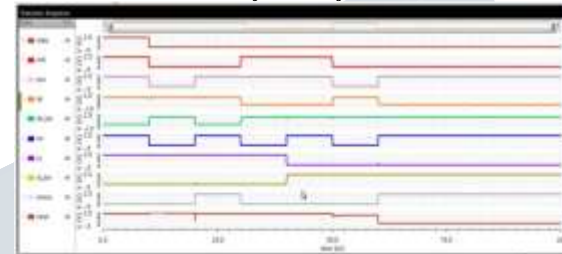
D. Read/ Write Waveforms of ST Based 11T SRAM



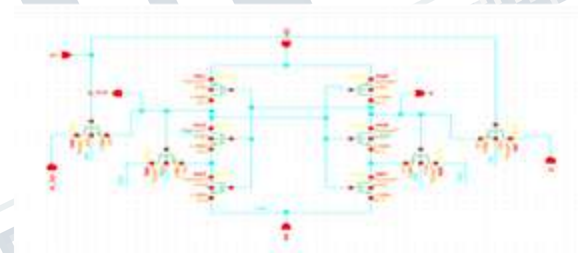
E. 6T SRAM Cell Schematic



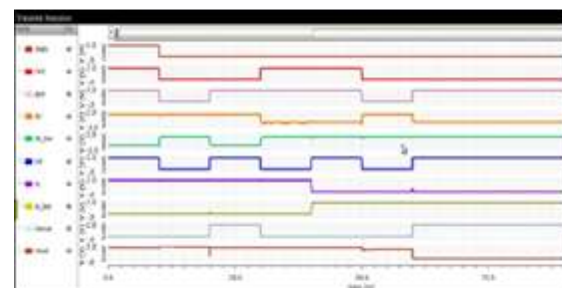
F. Read/ Write Waveforms of 6T SRAM Cell



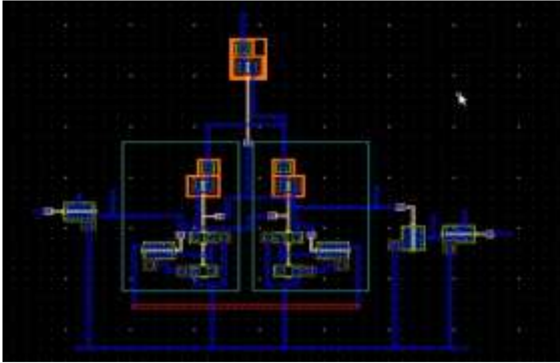
G. 10T SRAM cell Schematic



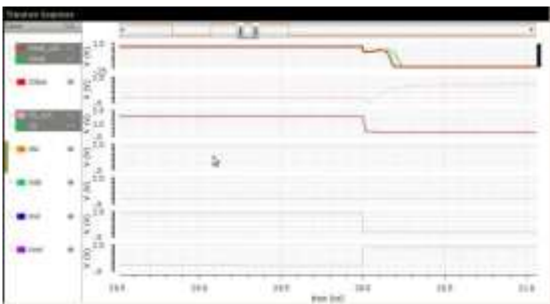
H. Read/ Write Waveforms of 10T SRAM cell



I. Layout of proposed 12T SRAM cell



J. LVS of proposed 12T SRAM cell



K. POWER COMPARISION TABLE

	Average Power	Leakage Power
Proposed 12T SRAM	0.8uw	0.28uw
11T SRAM	11.28uw	10.75uw
8T SRAM	43.75uw	43.13uw
7T SRAM	64.99uw	62.09uw
6T SRAM	10.3uw	4.09uw
10T SRAM	10.12uw	4.07uw

VI. CONCLUSION

In this work a Schmitt trigger based 12T SRAM is designed and simulated using cadence virtuoso with 180nm technology. The proposed design is a single ended SRAM configuration. Also the proposed 12T SRAM bitcell's average power and leakage power is calculated. both average power and leakage power of the cell has been compared with various other SRAM Configurations like 6T, 7T, 8T, 10T,11T and 12T. 6T and 10T SRAM Cells are operated differentially, but 7T, 8T, and 11T SRAM Cells are single ended SRAM Cells. The power comparison shows that the proposed 12T cell consumes lowest average power as well as leakage power. But the area has been increased due to the increase of no. of transistors compared to other SRAM cell's considered for comparison. Finally for the proposed cell both the design rule check and layout versus schematic has been verified.

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