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A Comparative Study of Low Power Transition, Area Overhead and Fault Coverage Testing Techniques for Digital Circuits

[1] Suhas B Shirol, [2] Rajashekar B Shettar
[1] Dept. of ECE, BVBCET, Hubballi, India

Abstract-— **In recent years, the technology is changing faster than the Moore's law stated hence to develop the devices which are efficient with respect to power, area and speed has become a challenge in field of VLSI. The main focus of this paper is comparative study of Low Power Transition, Low Area and High Fault Coverage in BIST architectures, it has been seen that during test power consumed is higher due to transition activity, area overhead is more and fault coverage is less for CUT.**

***Keywords*- Linear Feedback Shift Register(LFSR),Built In Self Test(BIST),Circuit Under Test(CUT), Low Transition LFSR.**

I. INTRODUCTION:

In current scenario , with the feature size being reduced in semiconductor manufacturing technology, the requirements of digital and analog Very-Large-Scale-Integrated (VLSI) circuits, which are poised of Million‟s of gates, have given rise to many challenges during manufacturing test [1]. The power dissipated is substantial during test data for the large and complex chips, which greatly increases the system cost [2].

The low correspondence among test vectors raise switching activity and eventually leads to power indulgence in the circuit. Built In Self Test (BIST) is the most appropriate approach for low power testing in digital circuits as it provides a large scope for low power techniques to be used. Test Pattern Generator for BIST is mainly using LFSR [3][4].

All possible test vectors with a proper use of tap sequence are generated using LFSR. The reordering techniques for test vectors aim to decrease the switching activity by modifying the order in which the tester applies the test vectors to the Circuit Under Test (CUT). Fault coverage is not affected by reordering of test vector, just their order is modified. Test cost can be reduced by improving use of test parameters [5].

II.LITERATURE SURVEY

A. Low Power Transition

One widespread method used to reduce test power consumption is the design of low transition TPGs. Most of these techniques amend LFSR design in such a way as to reduce the transitions in the inputs of the Circuit Under Test (CUT) for test-per-clock BIST or scan-chain for scan-based BIST.

Pattern Generator	*CUT*	*Power Consumption*	*Novelty*
LFSR	Digital Circuits	Reducing a switching activity	Designing a new structure of LFSR to generate more than one pseudo random bit per one clock pulse[6].
Clock Controlled LFSR	Memory	Reduction in switching activity to reduce power consumption	The address models are produced by a blend of LFSR and a 2- bit pattern generator (Modified LFSR) and two distinct clock signals[7].
BIST	ISCAS‟85 Benchmark Circuit	Reduce the power consumed by	A low power LFSR to reduce the power

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		reducing the switching activity	dissipation in test mode[8].
LP LFSR	A 4x4 Braun array multiplier	Reduces the switching activities between the test patterns	A novel TPG which is more suitable for built in self test (BIST) structures used for testing of VLSI circuits[9]
Accumulator based Weighted Pseudorandom BIST	C17 Benchmark Circuit	Switching behavior is reduced among the test patterns.	Testing of integrated circuits and systems using Pseudorandom built-in-self-test (BIST) generators have been widely utilized [10].
LT-GLFSR	ISCAS Circuits	Power consumption is reduced	A novel TPG technique called LT-GLFSR with BI and BS[11].
2D-LFSR	CMOS	Power consumption is reduced by nearly 70%	Low power 2D LFSR is proposed that reduces the weighted switching activity rate of the nodes of the CUT [12].
LP-LFSR.	Braun array multipliers 4x4 and 8x8	Reduces the switching activities among the test patterns	One of the most suitable Test pattern generator for (BIST) structures used for VLSI Circuit [13].
LT-PRPG	ISCAS"89 Benchmark Circuit	Reduces the number of transitions hence reduces switching activity	Novelty projected in this paper, LT-PRPG is poised of a LFSR and a 2x1 multiplexer[14].

Table A.1: Low Power Transition Survey

Here the survey for different pattern generation with Circuit Under Test(CUT) the result shows the reduced power consumption with novelty of work done shown in Table A.1 Low Power Transition Survey.

B. Area Overhead

Area overhead plays important role during the testing of BIST circuits. Here is the survey for different pattern generation with Circuit Under Test(CUT) the result shows the area overhead survey with novelty of work done shown in Table B.1

Pattern Generator	*CUT*	*Area Overhead*	*Novelty*
PLPF, Basic, Swap and Moving Approaches	ITC'99	Swap and Moving can be used for low area overhead	Novel power controlling method to control the switching between the patterns to an arbitary level by modifying pseudoTPG Test Pattern Generator) of logic BIST[15]
MLRTPG and A3WRTPG	CMOS	Reducing the area overhead by employing Adders and Dflip Flops	Power and Area overhead reduced[16].
Registers with non-linear update	Benchmark Circuit	With less area overhead and test time reduction	Registers with non-linear update for onchip generation of deterministic test patterns [17].
Clock Controlled LFSR	Memory	Area occupied by clock controlled LFSR is same as traditional LFSR.	Two distinct clock signals, LFSR and 2-bit pattern generator used to produce the address models [18].
MSIC TPG	ISCAS"85 and ISCAS"89 Benchmark Circuit	Low hardware and test overhead	MSIC vector are Generated by multiple single input change in a pattern [19].
Arithmetic BIST	ROM Modules	Logical time and slight hardware overhead.	Arithmetic BIST with Two-pattern test generator

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			is addressed in this paper [20].
LT-RTPG and 3-weight WRBIST.	ISCAS,,85 benchmark circuits.	Low hardware overhead.	can based BIST architecture with negligible hardware Overhead TPG [21].
Accumulatorbased Weighted Pseudorandom BIST	C17 Benchmark Circuit	Reduce the hardware implementation cost	Integrated circuits(IC) and systems are widely tested by Pseudorandom BIST generators [22].
March test Algorithm	Memories with BIST.	On the basis of area overhead March X,March LA is most efficient and March Y, March AB is the least efficient.	Different type of March algorithms are modeled for memory BIST[23]
3-weight weighted random BIST	Benchmark Circuits	Minimum hardware overhead	Serial Fixing BIST, Parallel Fixing BIST[24]

Table B.1: Area Overhead Survey

C. Fault Coverage

Pattern Generator	*CUT*	*Fault Coverage*	*Novelty*
PLPF, Basic, Swap and Moving Approaches	B22 benchmark circuit of ITC'99	More fault coverage without escalating test time.	Novel power controlling method to control the switching between the patterns to an arbitrary level by modifying Test Pattern Generator of logic Built In Self Test[15].
Registers with nonlinear update	Benchmark Circuit	Higher stuck-at Coverage	New technique for On-Chip generation of deterministic test patterns based on registers with non-linear update[17].
BIST	ISCAS"85 Benchmark Circuit	Considerable fault coverage.	A low power LFSR to reduce the power dissipation in test mode[25].
Arithmetic BIST	ROM Modules	Arithmetic module faults can be detected.	Two-pattern test generator for Arithmetic BIST is presented[20].
LT-RTPG and 3-weight WRBIST.	ISCAS,,85 benchmark circuits.	Fault coverage is high in this pattern generator.	A low hardware overhead TPG for scan-based Built-In Self-Test (BIST)[21].
Accumulator -based Weighted Pseudorando m BIST	C17 Benchmark Circuit	Fault coverage is more.	Pseudorandom BIST generators have been widely used to test integrated circuits(IC) and systems in digital VLSI[26].
Arbitrary Density Patterns (ADP)	S298 benchmark circuit	Decreases test length with increased fault coverage	Weighted random patterns and Transition density patterns are two Dynamic technique usage under adaptive switching of clock[27].
LT-GLFSR	ISCAS Circuits	This technique is used to find Stuck-at and transition faults in sequential circuits	A novel TPG technique called LT-GLFSR with BI and BS[11].
BS-LFSR	Benchmark Circuit	Detect all or most of the faults	Output pattern of LFSR to design LTTPG sequence [28].
Data background sequences(D BS), March SAM	Memory(SR AM)	Coupling Faults	Testing of SRAM's is more efficient with a memory BIST controller based

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			on FSM Architecture [29].
MemBIST, MARCH SAM Algorithm	Memory (RAM)	Single cell faults, Coupling faults	Comparison of Microcode based & FSM based MBIST controllers on the basis of logic usage and speed is done[30].
March Test Generator	Memory (RAM)	Static and dynamic faults, linked and unlinked faults, single and multiple port	tool for explaining the essentials of RAM, the tool has been used as an educational instrument for lab work[31].
3-weight WRBIST,LT -RTPG	ISCAS 89 benchmark	High fault coverage .	Almost 100% fault coverage for all standard circuits in VLSI[32].
DS-LFSR	ISCAS85 and ISCAS89 benchmark circuits	High fault coverage	Two linear feedback shift registers (LFSRs) are used to create DSLFSR [33].
3-weight weighted random BIST	Benchmark circuits	100% fault coverage can be predicted.	Proposed architecture can be implemented at low hardware overhead by using namely parallel and serial fixing BIST[24]

III. CONCLUSION

In this paper a qualitative survey on Low Power Transition, Low Area and High Fault Coverage in BIST architectures was carried out. The major area of concentration was on pattern generator and the Circuit Under Test with low power transition, area overhead and fault coverage for most of the testing techniques. Also we can see that some of the pattern generator can be used for low transition and area overhead or low transition and fault coverage. Novelty of the work carried out for different pattern generator is provided so that future work can be carried out in the field of BIST architecture for digital circuits.

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