Analysis of IR Drop, Signal Electromigration and Self-Heating Effect using Flat and Hierarchical Method in FinFET Technology

[1] Srinidhi KS, [2] Ravi HK

[1][2] Siddaganga Institute of Technology, Tumakuru, Karnataka, India
Email: [1] sriinnidi1999@gmail.com, [2] ravihk@sit.ac.in

Abstract— VLSI industry has been rapidly growing where multiple processors can be implemented on a single chip. In physical design of a chip main factors to be considered are timing closure, congestion, and power. Compare to 180nm and 90nm designs were not much complicated due to less transistor density as going to lower technology nodes chip size, area, length will decrease that impact on packaging and cooling issues, so it is necessary to estimate the power at the early stage of design. Power analysis is done immediately after placement and routing stage of the chip. Power analysis can be performed in two methods one is flat method and other is hierarchical method. In flat method of analysis, the data of both top level and block level is given as input data to calculate the results whereas in hierarchical method of analysis the Power Grid View (PGV) of hierarchical block is designed which is then given as input. In hierarchical runs the sub-blocks are black boxed. The simulation is carried out using the Voltus IC Integrity Solution tool from cadence for a chip designed in 16nm FinFET technology. The results obtained from the flat method of analysis takes 2X the runtime compared to hierarchical method which would be unfavorable for very much larger circuits. The IR drop in VDD and VSS are 11.69 mW and 11.02mW respectively in flat method and 12.32 mW and 13.26 mW for VDD and VSS in hierarchical method of analysis. The accuracy is more obtained in flat run due to its transparency in logic functions.

Index Terms— Fin-type Field Effect Transistors (FinFET), Signal electromigration (SEM), Self-Heating effect (SHE)

I. INTRODUCTION

Automation is a long-time idea that is stimulated in the minds, and this was the reason nowadays, we are living in an automated society, but still automation is not strongly developed in many other fields of technology. Development of design automation in technologies is unbelievable but we must believe in this because it has important to speed up the testing ways of these technologies before being used by human, to be sure about their performance which are considerable. For example, if we look at the IoT world which performs an important role in technologies to make the physical objects applicable, we will find out that they are error prone. One of the good examples to show how an error can impress on the client's satisfaction level is smartphones. Whenever we talk about speed, automation is pointed. In fact, Automation is an idea to turn from manual tests, which are sort of weak compared to the automatic ones. Higher speed of automatic techniques caused automation to play a significant and unique role in different technologies. Because manual ways have limited capacity for evolution, automatic methods can be the appropriate replacement. The growth of manual solutions toward software - driven ones can be called automation.

To include many logic functions into a single chip, designers are trying to customize chip based on the variety of applications. This leads to increase in density of the chips which gives rise to problems like process variations, thermal variations, packaging, cooling issues, etc. Different methods are considered at different levels to tackle these problems such as to reduce power dissipation, methods like scaling supply voltage or operating modules at different voltage supplies are considered at architectural level.

At transistor level scaling down the device size, reducing threshold limits are considered. Fin-type Field Effect Transistors (FinFET) is one such example where its device structure has the fin (channel) fully surrounded by gate on both the sides. FinFET's can be easily replaced by the bulk CMOS devices because it has a benefit like high ON and low OFF currents, low power consumption, high integration density and short channel effects are reduced.

In [1], hierarchical method of analysis is used for post-layout verification to reduce the verification time by considering IR drop and EM issues so in this paper both flat and hierarchical methods are performed, and hierarchical methods takes less run time compared to flat method. The hierarchical design can be approached by Top-down or bottom-up fashion. In [2], voltus tool and joule tool is compared with the percentage of leakage, switching and Internal power. From the voltus analysis, leakage and switching power are accurately measured. Later EM estimation is done on the optimized PDN by making sure the IR drop does not exceed 10% of VDD [3] and 10% of VDD will be assumed as initial IR drop of any node when the circuit is smaller than the critical value [5]. Effect of timing, temperature, interconnect technology scaling, barrier and defined thickness has been considered for the analysis of IR drop [4].

Figure 1 shows the general block diagram of power analysis. When a designed circuit consumes maximum current than the power supplied, the power supply can't provide a sufficient current and brings about voltage drop (IR drop) that will induce the circuit performance degradation. In deep submicron technology, IR drop is a common signal integrity issue.

IR drop mainly causes the circuit delay, but it will also minimize the circuit noise margins by the lower supply voltage that will leads to reliability issues and IR drop mainly comes when the current consumption in the unexpected peak's is higher than the original specifications of the circuit designs. When the current flow in the metal atoms is high, metal will starts moving from its original place to other place this metal displacement will causes open (void) or bulging (Hillock) of metal layer. This effect is called electromigration. Due to this effect are either short or open of the signal line or power line takes place. FinFETs have a short channel control and switching characteristics [6] and the device scaling can be extended to nano-scale regime. The heat dissipation in FinFET is poor because of phonon boundary scattering that may cause Self-Heating Effect in circuit operations [7].
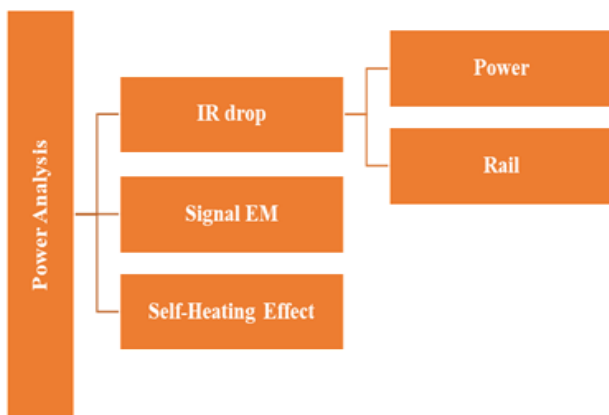

Figure 1: General block diagram of power analysis

II. METHODOLOGY

This section deals with the voltus tool setup for the estimation of power after the placement and routing stage. The inputs required for the IR drop, SEM, SHE analysis, and Power Grid View (PGV) creation and the steps carried out to perform flat and hierarchical method of IR drop analysis.

A. Inputs Required

- . v file -Gate level netlist
- . lef file-Library Exchange Format
- .def file - Design Exchange Format
- .lib file- Liberty Timing File
- .sdc file - System design constraints
- Common Power Format
- .spef file - Standard Parasitic Exchange Format
- Power Grid View

B. Flat Method

In the traditional flat analysis flow, the entire design data is given as input for Power analysis to perform power calculation and generate current files. These current files, along with the complete design and power grid views of primitive cells, are used as input for rail analysis to generate IR drop results.
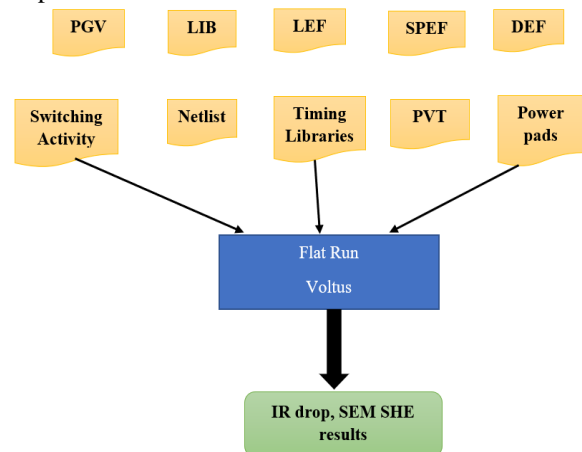

Figure 2: Flat run method flow diagram

Figure 2 explains the steps carried out to perform flat method of IR drop analysis. Flat method analysis provides the accurate results because it is transparent down to the logic cells, but it requires more memory and a significant amount of time to run because every cell and every wire in the design is analyzed.

C. Hierarchical method

For the hierarchical rail analysis, requires the flat or hierarchical current files, top-level design data, and PGV of hierarchical blocks and primitive cells. This flow does not require block level design data, instead it requires the PGV of hierarchical blocks. Therefore, the design information required for Rail analysis is very less. Thereby hierarchical flow provides the flexibility and scalability to perform static and dynamic rail analysis on very large designs with fast turnaround time
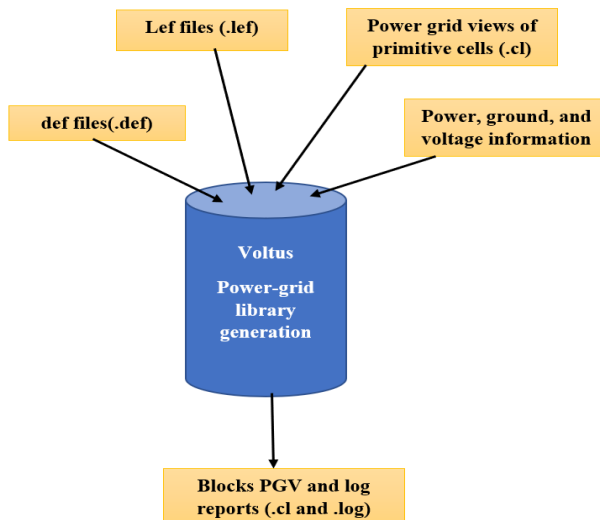
.

Figure 3: Block diagram of hierarchical PGV generation.

Figure 3 shows the block diagram for generation of hierarchical Power Grid Views. The hierarchical PGV generation of a block is part of the top-level hierarchical rail analysis. The inputs for hierarchical PGV generation are DEF and LEF files for the hierarchical blocks, PGVs of primitive cells, power, and ground information of the blocks.
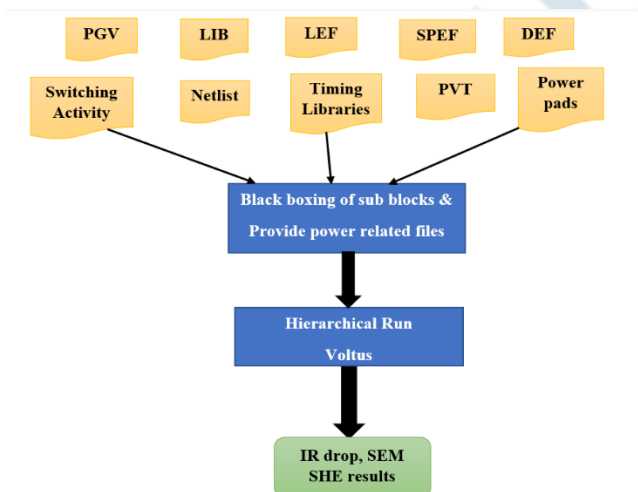

Figure 4: Hierarchical run method flow diagram

Figure 4 briefs about the hierarchical method of analyzing IR drop, Signal Electromigration (SEM) and Self Heating Effect (SHE). A top-level of chip is considered to perform hierarchical IR drop analysis. The following steps describes the hierarchical analysis flow:

- To load the Top-level hierarchical design. Specifying the block-level Verilog, DEF, primitive cell's LEF and block level LEF files in the design.
- To ensure that there are no connectivity violations around the block.
- To perform hierarchical PGV generation.

- Run static/dynamic rail analysis.

Due to resistive power grid or simultaneous switching of close instances, there is reduction in voltage on VDD nets and increase in voltage on VSS nets. The IR drop analysis is so important because the resistance increases with advanced nodes, and power increases with high operating frequencies, both resulting in IR drop violations. IR drop may cause timing issues if they are higher than 5%‐10% of effective supply voltage or cause functional failures if they are more than 20%‐30% of effective supply voltage.

III. RESULT AND ANALYSIS

The post layout IR drop, SEM and SHE verification is performed using flat and hierarchical method. The simulation was performed using the 'Voltus' Tool from cadence. The foundry limit for IR drop is below 20mV and, bump currents to be less than 300mA.

A. Flat Run Method Results of IR Drop

In flat method of analysis all the inputs related to every sub‐block are given as input along with the top related information. The chip is always checked in worst scenarios to work in all possible conditions of Process, Voltage and Temperature. The fast-fast corner is used for process with 0.86Mv voltage and a temperature of105°.The reports of IR drop analysis of VDD and VSS is done separately for better analysis. The table I shows the flat run results of IR drop and SEM analysis. The run time in Flat method for IR drop, SEM and SHE analysis was around 15hrs, 5hrs and 20 hrs, respectively. The total power consumed by the chip according to flat run analysis is 3976.6 mW in which 9.3% is of leakage power, 31.77% is of switching power and 58.91% is of internal power.

Table.1 Results of flat run

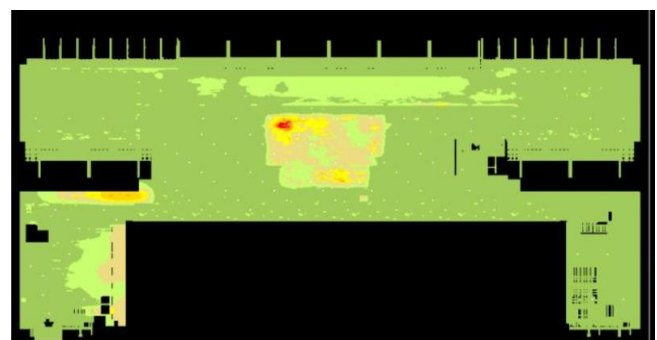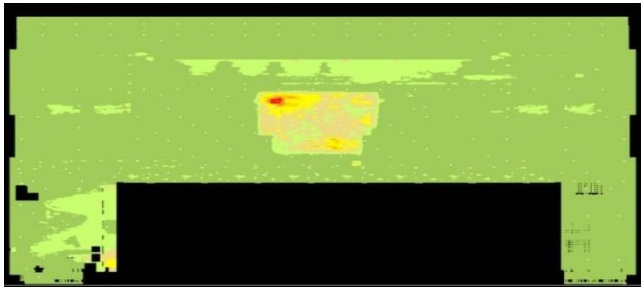|	VDD	VSS
IR Drop	11.69 mV	11.02 mV
Bump currents	222 mA	189 mA
PGEM Violations	1	34

Figure 5: IR drop of VDD in flat method

Figure 6: IR drop of VSS in flat method

B. Hierarchical run method results

In hierarchical method, the power analysis is performed on each sub-block and the power files of all sub-blocks are added as input. The reports of IR drop analysis of VDD and VSS is done separately for better analysis. The table II shows the hierarchical run results of IR drop and SEM analysis. The run time in hierarchical method for IR drop, SEM and SHE analysis was around 7hrs, 3hrs and 14 hrs, respectively. The total power consumed by the chip according to flat run analysis is 3405.6 mW in which 8.7% is of leakage power, 14.56% is of switching power and 76.69% is of internal power.

Table 2: Results of Hierarchical Run

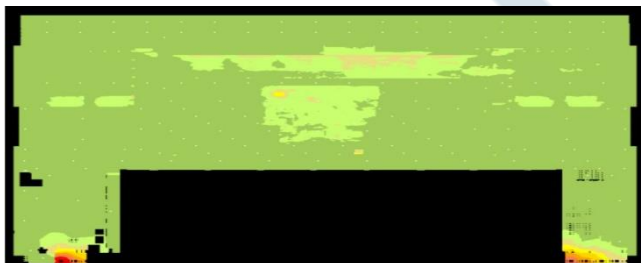|	VDD	VSS
IR Drop	12.32 mV	13.26 mV
Bump currents	202 mA	295 mA
PGEM Violations	1	34

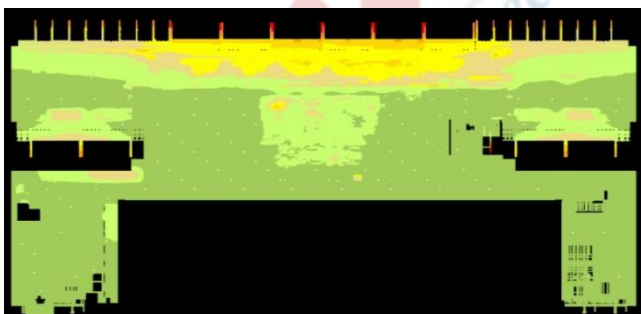**Figure 7:** IR drop of VDD in hierarchical method

Figure 8: IR drop of VSS in hierarchical method

The percentage of error for common set of resistors between two runs is calculated by Percentage of error = ((IR hier−IR flat) / IR flat)* 100 -(1)

Substituting the IR drop values from flat and hierarchical method of run, we obtain 5.39% of VDD and 20.32% of VSS as error. The run time in hierarchical method was almost half of that used for flat run. It is seen that the results obtained are all within the limit range defined. Also, the IR drop values of flat run method is much more accurate than hierarchical, but it requires a substantial amount of time. Power and rail analysis reviews are done by analyzing logs and reports. Different *.gif files like ir*.gif to view IR drop, rj.gif to view PGEM violations, grid_unconnected.gif to view unconnected metal segments, pv.gif to view voltage drop overpower gate, etc. are analyzed and reviewed.

SEM generates a report with Irms/Limit, Ipeak/Limit and Iavg/Limit which specifies the RMS current, peak current and average current value respectively that flows through the metal/via resistor that is calculated by the tool divided by the current limit value provided by foundry. Figure 9 shows the EM violation summary. In this implementation the values of PGEM violations were not varying much than the specified limit(10). So, the violations existing could be ignored.

Figure 9: Result of EM violation summary

SHE run computes RMS currents on signal wires and on power network wires and generates Detail Delta Temperature (ddt) file, Instance Delta Temperature (idt) file and Tile Delta Temperature (tdt) file. The ddt file reports the increase in temperature for all metal layers in the entire design and the idt file reports the increase in temperature for all instance in the entire design. In this experiment there were no instances reporting increase in temperature and were all within the specified limit.

IV. CONCLUSION

The analysis of IR drops, signal electromigration and self-heating effect of a chip designed in 16nm FinFET Technology is performed. The results obtained are reviewed and the tradeoff between accuracy and run time is noted. The runs are carried out using the Voltus tool from Cadence. The hierarchical method run times were almost half the time taken by flat method. The IR drop of the chip was about 12.326 mV in hierarchical method and 11.69 mV in flat method for VDD. For VSS it was 13.26 mV in hierarchical and 11.02 mV in flat method. There was 1 and 34 electromigration violations in VDD and VSS respectively in both flat and hierarchical methods. As the values were slightly more than required limit, it could be neglected. Also, there was no violations of Self-heating effect. The total power from hierarchical to flat had a percentage error of 5.39 (VDD) and 20.32 (VSS). The results show us that hierarchical method of

post layout verification is much simpler, easier, and faster when compared to the flat run.

REFERENCES

[1] Tarjina Islam, "A Hierarchical Method to Perform IR Drop and Electromigration Analysis for Faster Tape-out of Analog-on-Top Designs", Conference: ANALOG 2018 - 16. GMM/ITG-Fachtagung, München/Neubiberg, Deutschland, Sep 2018, ISBN 978-3-8007-4754-2.

[2] Ranjith H V, Sujatha Hiremath, Saya Goud Langadi,"RTL power estimation: Early design cycle approach for SoC power sign-off," 2018 IEEE International conference on recent trends in electronics, Information & communication Technology (RTEICT-2018).

[3] S. Dey, S. Dash, S. Nandi, and G. Trivedi, "PGIREM: Reliability-Constrained IR Drop Minimization and Electromigration Assessment of VLSI Power Grid Networks Using Cooperative Coevolution," 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Hong Kong, 2018, pp. 40-45.

[4] Vanpreet Kaur, "IR Drop Analysis and Its Reduction Techniques in Deep Submicron Technology",Int. Journal of Engineering Research and Applications, ISSN: 2248- 9622, Vol. 5, Issue 1(Part 4), January 2015, pp.55-62

[5] V. Sukharev, X. Huang, H. Chen, and S. X. -. Tan, "IR-drop based electromigration assessment: Parametric failure chip-scale analysis," 2014 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Jose, CA, 2014, pp. 428- 433.

[6] S. E. Liu, J S Wang, Y R Lu, D S Huang, J H Lee. "Self-heating effect in FinFETs and its impact on devices reliability characterization," 2014 IEEE International Reliability Physics Symposium, Waikoloa, HI, 2014, pp. 4A.4.1-4A.4.4.

[7] Claudio Fiegna, Yang Yang, Enrico Sangiorgi, Anthony G. O'Neill." Analysis of Self-Heating Effects in Ultrathin-Body SOI MOSFETs by Device Simulation." IEEE Trans. Electron Devices, vol.55, no.1 pp.233-244, Jan 2008