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Automation Checks during PNR flow in IC Design

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Abstract*— Automation is a technology in that there are different kind of approaches and procedures can be referred. The process of turning manual checks to automatic checks provides impressive benefits. Time saving, cost effective, higher quality, accurate result, less error in the tests which normally caused by human are the most important reasons to thinking about automation. The first and foremost step is to find out what should be automated. It is important to know the reason of automation if, it is worth or not. Here, the question is based on which reason it should decide for automation? For instance, after finishing all the runs of Innovus, Voltus, Pegasus, Quantus top level person must verify that whether it is meeting the specifications or not for checking that they need to go through all the audit files. Audit files doesn't contain detailed information's like incremental tag, tool version, time stamp, md5sum's, waivable warnings, must fix warnings, must fix errors, input directory paths, Bump locations and VDD and VSS locations etc. and other factor is Time consuming. By doing automation it will gives required detailed information like latest incremental tag and tool version, md5sum its unique id, time stamp, errors, warnings, setup and hold views etc. so it can be automated by developing script using programming language called TCL (tool command language). These scripts will work for any block of a chip which is of 16nm technology.

***Index Terms*— Tool Command language (TCL), Placement and Routing (PNR), Innovus, Quantus, Pegasus**

I. INTRODUCTION

Automation is a long-time idea that is stimulated in the minds, and this was the reason nowadays, we are living in an automated society, but still automation is not strongly developed in many other fields of technology. Development of design automation in technologies is unbelievable but we must believe in this because it has important to speed up the testing ways of these technologies before being used by human, to be sure about their performance which are considerable. For example, if we look at the IoT world which performs an important role in technologies to make the physical objects applicable, we will find out that they are error prone. One of the good examples to show how an error can impress on the client's satisfaction level is smartphones. Whenever we talk about speed, automation is pointed. In fact, Automation is an idea to turn from manual tests, which are sort of weak compared to the automatic ones. Higher speed of automatic techniques caused automation to play a significant and unique role in different technologies. Because manual ways have limited capacity for evolution, automatic methods can be the appropriate replacement. The growth of manual solutions toward software - driven ones can be called automation.

Figure 1 shows the general flow of Automation process . The main aim of this automation is to verify the correctness of input used, and to make sure that post layout documentation is exhaustive ,and to save the time for analyzing the reports . In [1], the issues involved in TCL that is debugging TCL code, detecting syntax errors, and what will happen when TCL is busy for several times. In addition to that TCL becomes the choice of developers to interface with EDA tools, waveform analysis, synthesis and it has good control over GUI based simulations are considered. Automation operations replaces the manual operations by using tools and scripts and new automation can also be developed just by modifying smaller things in the scripts[2] and automation reduces future maintenance effort , reduces cost [3][4] and improves quality.

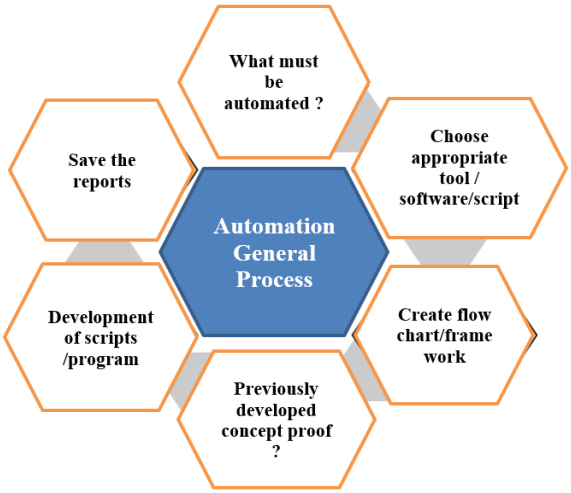

Figure 1: General flow of Automation Process

II. METHODOLOGY

This section deals with the script development and flow chart of the scripts developed .

A. Script development

Four scripts are developed that employed standard automation design techniques to extract information related to audit files.

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Table 1: Design Automation in Design Environment

Automation	Main Topic	User inputs	Outputs
Script #1	Write a script that will generate required information of Innovus checklist. (Checklist provided in the Innvous audit file)	Block name & Directory path	Information related to Floorplan, Power plan, CTS, Placement, Routing.
Script #2	Write a script that will generate required information of Voltus checklist. (Checklist provided in the Voltus audit file)	Block name & Directory path	Information related to IR drop, SEM, SHE.
Script #3	Write a script that will generate required information of Physical verification (Pegasus) checklist. (Checklist provided in the Pegasus audit file)	Block name & Directory path	Information related to LVS, DRC, MSCC, Antenna.
Script #4	Write a script that will generate required information of Quantus checklist. (Checklist provided in the Quantus audit file)	Block name & Directory path	Information related to DEF, DBS, STA, CLP, LVS, GDSII, Metal Fill, Unconnected nets, Tielo nets.

The script is written in such a way that it can work for any block in a 16nm chip just by changing block name and working directory path of the block.

User Inputs:

1. Working Directory path
2. Information storing Directroy path
3. Block Name

B. Flow chart to create working directory and folder

User has to enter the directory path from which it has to get the required block information and this assigned to common variable and after getting the information it has to store in one common directory location for the analysis It is also accessed by common variable and it will create the file as read and write mode if that file is already created then again it will not create the file.

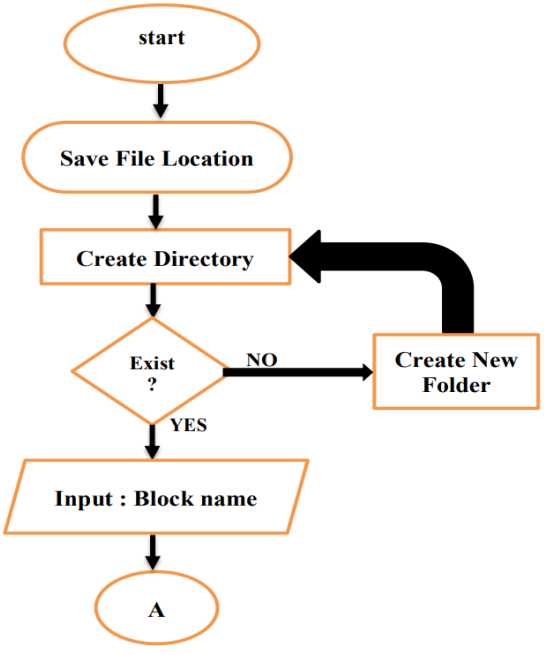

Figure 2: Flow chart to create directory and folder

C. Flow chart for the power analysis

Creating directory is general process for all Voltus, Innovus Pegasus, Quantus. Voltus is for doing power analysis in that there are two kind one is directly doing IR analysis and other is doing power analysis then doing Rail analysis two step that comination is IR analysis. So if only IR analysis is performed logs and output reports will be generated for IR analysis in that it includes power and rail analaysis information and if Power analysis is performed it will generates separate output reports and logs for rail and power . So user has to specify whether it IR or Power in the script.

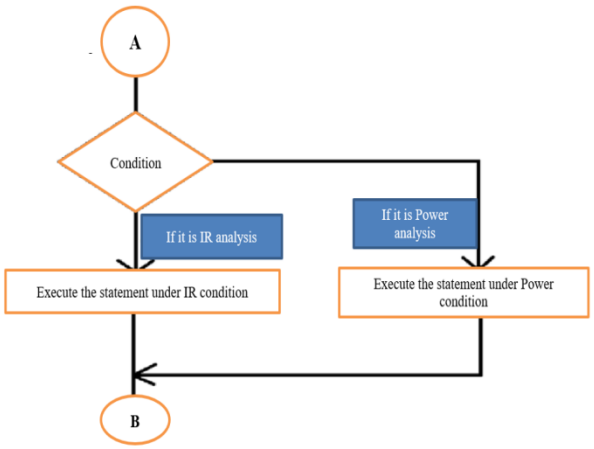

Figure 3: Flow chart to select the analysis is IR or Power

Above flow chart shows the condition to check for IR /Power analysis after checking the condition it will execute the statements then it will generates required information with respect to IR /Power .

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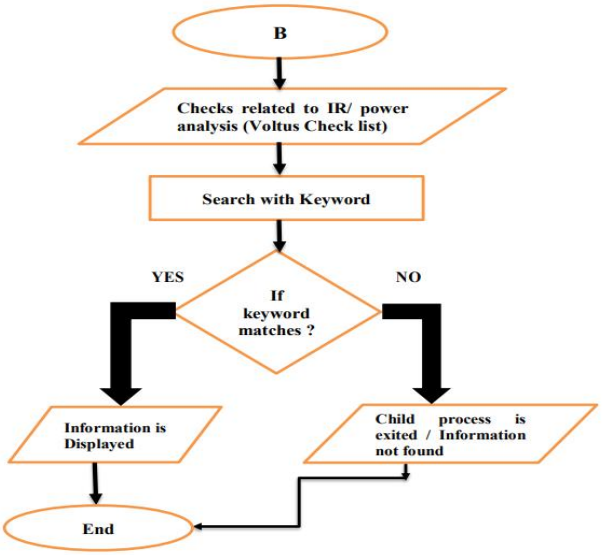
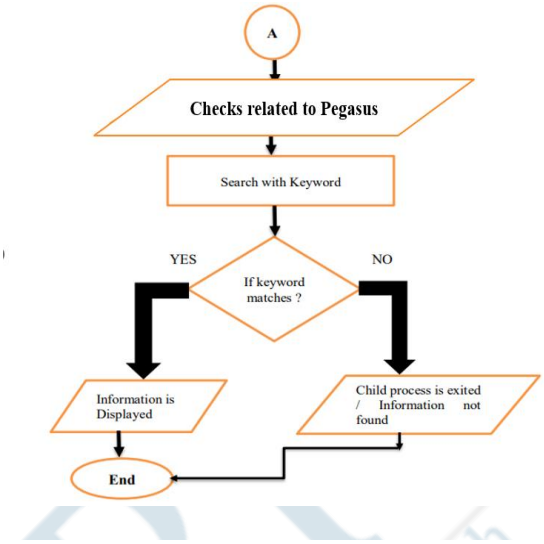


Figure 4: Flow chart of voltus checks related to power analysis

The above flow chart shows that how it will check the The above figure 4 flow chart shows that how it will check the required information mentioned in Voltus audit file. The information checks include md5sum of spef ,def, sdc ,PVT corner ,SDC path location Bump location of VDD and VSS , spef path ,abstract lef ,time stamp ,current tap percentage ,VC report ,main report ,waivable warnings ,must fix errors and waivable errors ,PGEM violations , Hold and setup views ,IR drop, VDD and VSS PG nets ,Disconnected instance ,Idt report ,skipped nets in SEM , Temperature corner used in SEM ,SEM violations etc.,. It will check with key word if it searches with respective keyword, it will display the required information if it is not found it will display command not found or child process exited.

D. Flow chart for the physical verification

Below Figure 5 flow chart shows that how it will check the required information mentioned in Pegasus audit file. The information checks include file versions of DRC,LVS ,V2LVS,MSCC, Antenna, time stamp of GDSII ,DRC ,LVS, final time stamp of LVS, V2CDL ,options used for DRC and LVS related to user net label ,exclude cell list, virtual connect ,select foundry checks ,DRC and LVS Tech data version ,DRC after cod fill, Results checks of TSMC, MSCC,DRC, Antenna DRC LVS result ,LVS run summary and extra pins source path checks, MIM cap layer. It will check with key word if it searches with respective keyword, it will display the required information if it is not found it will display command not found or child process exited.



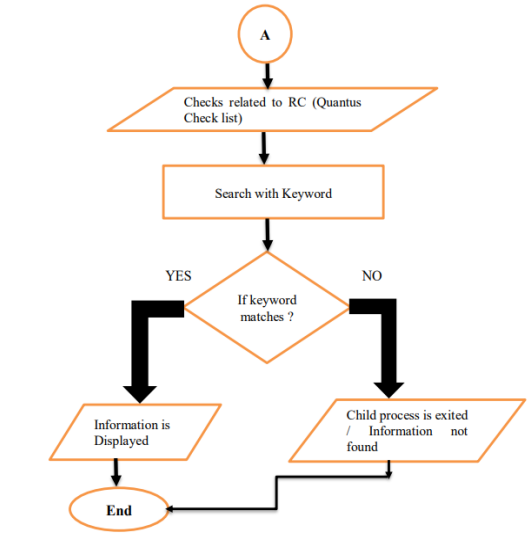


Figure 6 : Flow chart of RC parasitic extraction checks

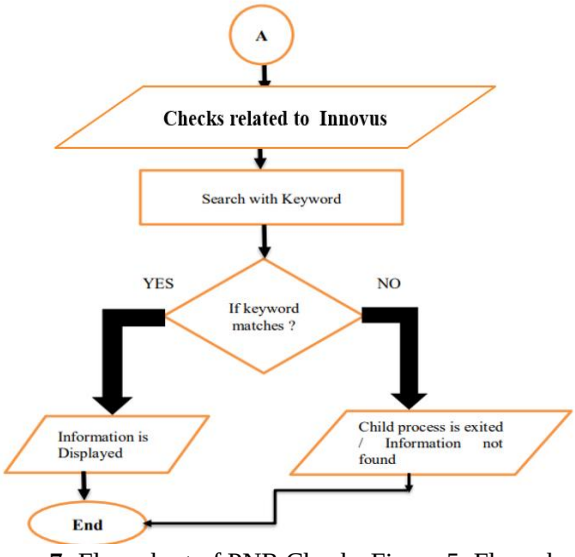


Figure 7: Flow chart of PNR Checks Figure 5: Flow chart of physical verification checks

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E. Flow chart for the RC parasitic extraction and PNR checks

Figure 6 flow chart shows that how it will check the required information mentioned in Quantus audit file. The information checks include QRC version, Input data sanity check includes verifying all files were written out from final database of DEF, DBS, STA, CLP, LVS, GDSII from final DBS, GDSII time stamp , time stamp of input files Verilog ,DEF, GDSII, Checking if SPEF was written out after final DEF generation, Fina DEF ,SPEF, Hierarchical metal fill gds used in config file and qrc , confirm metal fill gds used from tech file and from log ,warnings ,errors, mds5sum of audit tracker qrc and GDSII audit tracker . It will check with key word if it searches with respective keyword, it will display the required information if it is not found it will display command not found or child process exited.

Figure 7 flow chart shows that how it will check the required information mentioned in Innovus audit file. The Innovus checks include Innovus template version ,Directory structure used for block implementation ,Foundry specific settings of qrc and qrc tech file to match both outputs are same for qrc ,Stream out map file for chip level and block level ,CTS cell list used in design includes inverter cells, buffer cells ,logic cells ,clock gate cells ,setup views for init stage .preplace stage, place stage ,MBR stage ,cts ,route ,post rout ,dfm ,Hold views for CTS ,route ,post cts ,post route, dfm ,Analysis views for init stage and setup for init from database , Database and log match for init stage and setup views at preplace ,place, mbr, cts, similarly Hold views ,Database and log matches for poatcta setup and hold views similarly for post route setup ,comparison between database and log ,analysis views from config file ,setup and hold view comparison ,preferred hold cell list for postcts, route, postroute, dfm, clock layers PG pins (power and ground), verify connectivity at route , postroute, DFM, list of don't use of ECO gate array cells ,Route checklist involves DRC violations ,multi-cut via coverage ,clock shield percentage, errors.

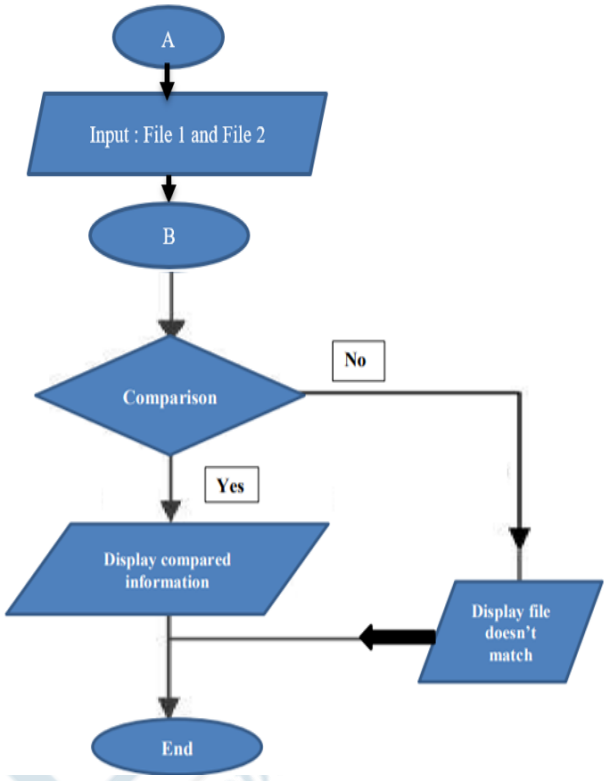

Figure 8: Flow chart of file comparison

III. RESULTS

The Automation results of power ,physical verification ,RC parasitic extraction and placement and routing results are shown in below figures .

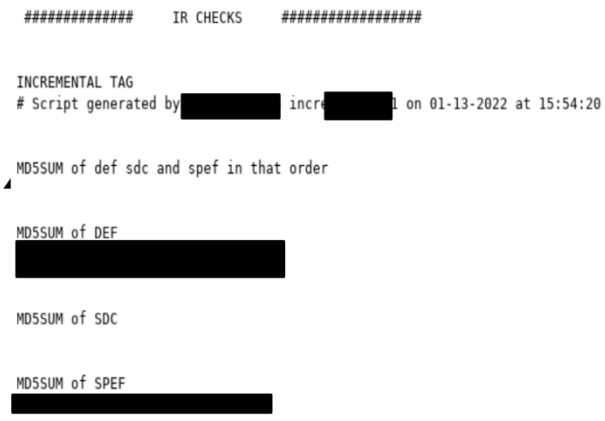

Figure 9: Voltus Checklist

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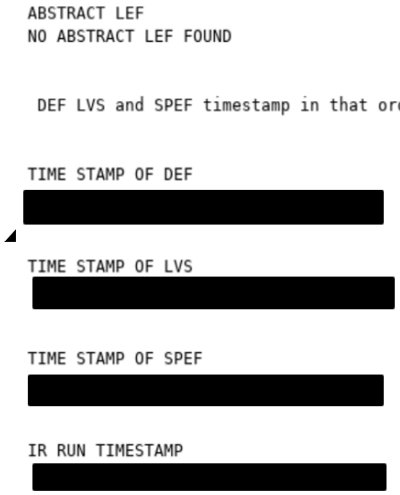

Figure 10 : Voltus abstract lef ,time stamp

Figure 11: Quantus results

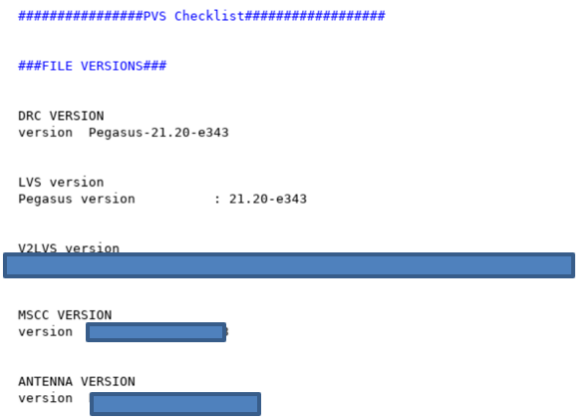

Figure 12: Pegasus reults

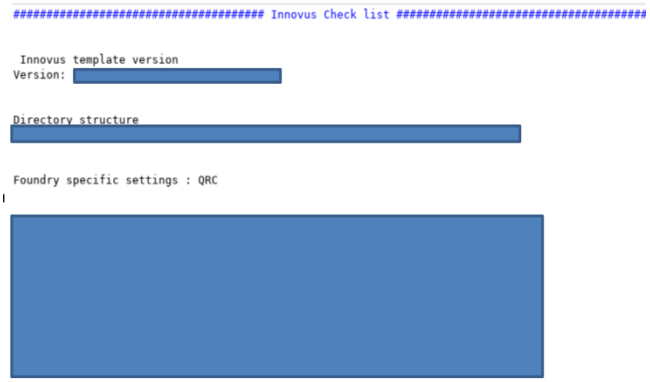

Figure 13: Innovus results

IV. CONCLUSION

After doing all the runs of Innovus, Voltus, Pegasus, Quantus ,analyzing of each report of different blocks becomes easy because of automation scripts it will grep the required information just by changing working directory path and block name. so, it gives required information in precise readable format. So, by doing Automation for different technology node, it will reduce human effort to check the required information manually (accessing individual logs and reports).

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