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A Nonvolatile 7T2M SRAM Cell with Improved Noise Margin for Energy-Efficient In-Memory Boolean Computations

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Abstract*— The current computing systems are facing von Neumann bottleneck (VNB) in modern times due to the high prominence on big-data applications such as artificial intelligence and neuromorphic computing. In-memory computation is one of the emerging computing paradigms to mitigate this VNB. In this paper, a memristor-based robust 7T2M Nonvolatile-SRAM (NvSRAM) is proposed for energy-efficient In-memory computation. The 7T2M NvSRAM is designed using CMOS and memristor with a higher resistance ratio, which improved the write margin by 74.44% and the energy consumption for read and write operation by 5.10% and 9.66% over conventional 6T SRAM at the cost of increment in write delay. The read decoupled path with the VGND line enhances the read margin and read path Ion/Ioff ratio of 7T2M NvSRAM cell by 2.69× and 102.42%, respectively over conventional 6T SRAM. The proposed cell uses a stacking transistor to reduce the leakage power in standby mode by 64.20% over conventional 6T SRAM. In addition to the normal SRAM function, the proposed 7T2M NvSRAM performs In-Memory Boolean Computation (IMBC) operations such as NAND, AND, NOR, OR, and XOR in a single cycle without compute-disturb (stored data flips during IMC). It achieves 4.29-fJ/bit average energy consumption at 1.8 V for IMBC operations.

***Index Terms*— Computing System, In-Memory Computation, Energy-Efficiency, Memristor, Robust SRAM, Von-Neumann Bottleneck**

I. INTRODUCTION

He state-of-the-art computing system based on Von Neumann architecture [1] suffers from Von Neumann Bottleneck (VNB) which hinders the further development of high performance and energy-efficient computing system. The conventional Von Neumann architecture has a separate unit for storage and computation, as shown in Figure 1(a). This physically separated memory and computation unit result in large energy consumption for data transfer between these two units. There have been many attempt for evaluation in a computing paradigm to overcome this van-Neumann bottleneck and energy inefficiency. To suppress the Von-Neumann bottleneck and to minimizing the energy consumption, In-Memory computations has been recently used in a computing system where data processing inside memory. In-memory computing system [2] has integrated computation unit (ALU) and memory unit as shown in Figure 1(b), which eliminate the energy consumption due to frequent data transfer operation between memory unit and ALU. In-memory computations has a huge impact on a computing system for a futuristic application like artificial intelligence, neuromorphic computing machine learning [3] - [4].

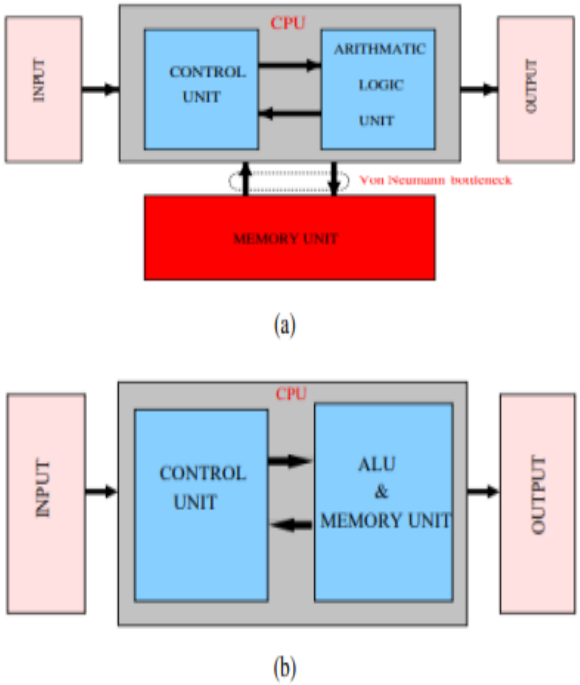

Figure 1: a) The conventional computing system with an illustration of the Von-Neumann bottleneck. b) The IMC system with an illustration of computational memory and ALU.

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Volume 9, Issue 1, Jan 2022

Due to IMC's significant impact on the future computing system, various research proposals traverse right from conventional CMOS to beyond CMOS technology have been analyzed in the literature. The several CMOS based IMC implementations have been proposed, recently with most of the approaches using convention 6T (C6T) SRAM [5]-[6]. For example, [5] reconfigured a C6T SRAM cell as a content addressable memory (CAM), TCAM, and SRAM memory and enabled bit-wise logic operation, while [6] demonstrated the IMC operation and developed a machine learning classifier using 6T SRAM. The 6T SRAM cell has a read-write couple path that increases the probability of read failure and compute disturb (store data flip during IMC) [7], when multiple rows of SRAM array activate simultaneously to perform In-Memory Boolean Computation (IMBC) operation, which leads to the design of a new SRAM cell that has a separate read and writes path. A 4+2T SRAM cell based on a deeply depletion channel (DDC) technology [8] has been proposed for IMC and searching application, which has a separate read and write path. However, this proposed cell performed an IMBC operation on store data in the peripheral circuit, which an extra write needed cycle to write back the computed result into the SRAM array that increased the system's latency. Thus [9] has proposed a novel read computation scheme along with the 8T SRAM and 8 +T SRAM cell use for enabling IMBC operation and store computed results into SRAM array in a single read-compute cycle. The 8T SRAM still suffers from low efficiency for large array sizes and compute-failure (provides false computation results in IMC).

The above-stated pieces of literature only focus on CMOS based SRAM cells to implement IMC. CMOS technology suffers from scaling issues and produces a larger leakage current at the scaled node [10], which affects the system's performance. But the state-of-the-art requirement is to develop high density and low power computing systems for the futuristic application. The memristor [11] is one of the emerging devices that can be used to design a computing system with high density, low latency, and energy efficiency [12].

In this paper, an energy-efficient 7T2M NvSRAM bit-cell is proposed. The proposed 7T2M NvSRAM improves read/write stability, leakage power, read delay, and energy with higher write delay when compared to C6T. The IMC operations can be easily implemented with the help of the proposed 7T2M NvSRAM bit-cell due to the following factors.

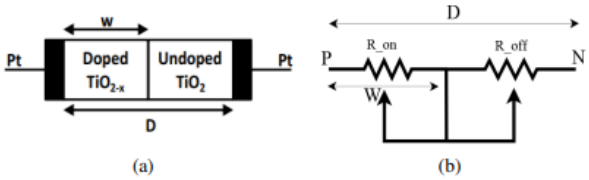

Figure 2: (a) The Device structure of Memristor. (b) The equivalent circuit of Memristor.

- IMC can easily be enabled by the read decouple path.
- These cells also provide significant read margin and write margin, so read disturbance, compute-disturbance, and half-select issues do not occur during the activation of multiple rows simultaneously inside the memory array

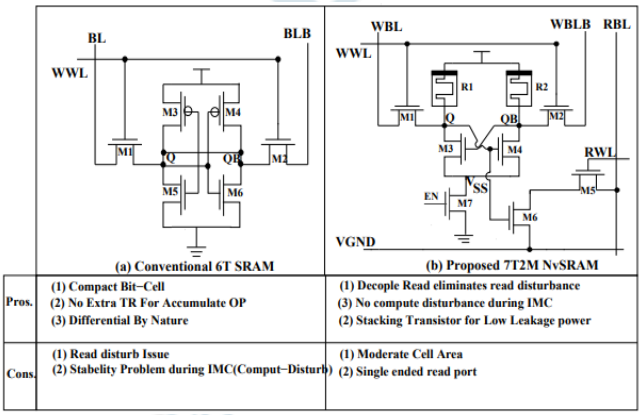

Figure 3: Comparison of C6T, and Proposed 7T2M NVSRAM.

The remaining of this paper is organized as follows, Section II presents the structure and characteristics of the memristor device for circuit simulation, Section III gives the overview of the structure of proposed 7T2M NvSRAM and write, restore and read operation, Section IV discusses the simulation result of the proposed 7T2M NvSRAM bit-cell and Section V presents IMBC in 7T2M NvSRAM bit-cell, Section VI presents analysis of NvSRAM-IMC, and final section VII presents conclusion and future work.

II. MEMRISTOR DEVICE

In this section, the working and structure of the memristor device are explained. In 1971, L.Chua theoretically [13] found out the fourth fundamental two-terminal electrical element memristor besides other three basic element such as resistor, capacitor and inductor. Initially, memristor is theoretical component but later on 2008, William at. all [11] has been physically implemented the memristor device. The titanium oxide (Tio2) layer is used as resistive material in physical memristor which is sandwiched between platinum (Pt) electrode as shown in Figure 2(a). The Tio2 layer is divided into two region: Oxygen deficient doped region (Tio2−x) act as conductor and undoped region (Tio2) act as insulator. The equivalent circuit representation of memristor is shown in Figure 2(b). The oxygen deficiencies of the

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Volume 9, Issue 1, Jan 2022

doped TiO2−x layer move toward the undoped region TiO2 when a positive voltage is applied across the doped side of the memristor. It increases the width of the TiO2−x layer, causing the lowering of memristor resistance. The memristor behaves as a Low Resistance State (LRS) in this condition. Conversely, if a negative voltage is applied across the memristor, it will attract oxygen deficiencies, increasing the width of the undoped region TiO2. This state of the memristor is known as the High Resistance State (HRS). If no voltage is applied across the memristor, the oxygen deficiencies will remain at their position; this is how the memristor remains in its previous state. Memristor is characterized by Verilog-A language for circuit simulation. Table I shows the physical and fitting parameters use for circuit simulation.

Table I: Memristor Device Parameters

Parameter	Definition	Value
HRS(*Ron*)	Memristor's maximum resistance	150 KΩ
LRS(R_{off})	Memristor's minimum resistance	20 Ω
D	Device size	10nm
μv	mobility of oxygen atom	$10 \times e{-}14\ m2V{-}1S{-}1$

III. THE PROPOSED 7T2M NVSRAM BIT-CELL

7T2M NvSRAM cell is designed to improve read/write margin, low static power during off state, and energy efficiency for IMBC. The proposed 7T2M NvSRAM cell is shown in Figure 3(b). It has seven transistors and two memristors. The two transistors (M3, M4) and two memristors (R1, R2) with V VSS are formed the core of the proposed bit-cell, where information is stored in-term of the memristor resistance state, and the other four transistors (M1, M2, M5, M6) are set as an access transistor. The proposed cell has a double ended write using M1 and M2 and a single-ended decouple read with VGND signal using M5 and M6 transistors. The proposed 7T2M NvSRAM has a lower impact on the storage node due to the read decouple path. Therefore read margin is significantly improved at cost of only 6% area overhead when compared to C6T. The VGND signal is used at read path to improve the Ion/Ioff ratio and also reduce the leakage current in read path. The transistor M7 is used to provide a stacking effect in 7T2M NvSRAM to reduce power for write, read, and off-state conditions.

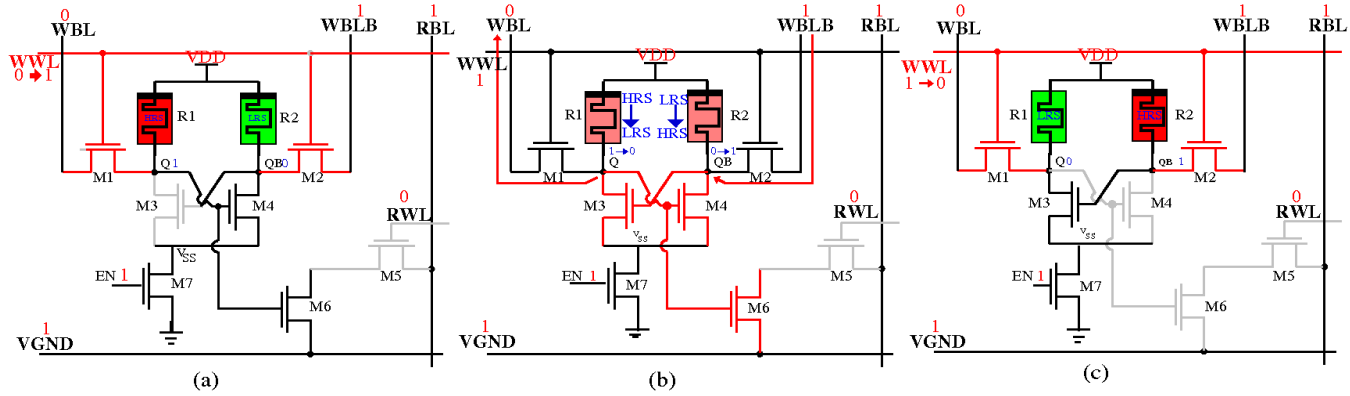

Figure 4: A series of the write operation process of the proposed 7T2M NvSRAM bit-cell shows writing '0' to node Q storing '1' initially. (a) The '0', '1', and '1' are asserted at WBL, WBL, and WWL, respectively, to write '0' at node Q and '1' at node QB. (b) The node Q and QB write and change the resistance state of R1 and R2. (c) The node Q hold '0' and QB hold ' 1'and reset the WWL to finish the write operation.

A. Write Operation

The write method of the proposed 7T2M NvSRAM is the crucial feature of this design. During the write operation, the RWL is kept at GND, VGND drive to VDD, RBL is kept at VDD, and EN signal is kept at high. For a write '1' operation into a cell, the WBL and WBLB are loaded with the value of 1 and 0, respectively, via write driver. Now WWL drives from GND to VDD to switch on the access transistors. The internal storage node Q and QB charged and discharged via access transistor M1 and M2, respectively. The memristor R1 and R2, connected to the drain terminal of M1 and M2, respectively.

Figure 4 illustrates a series of processes for writing a 0 to storage node Q in terms of the resistance state of the memristor device R1. The initial storage node Q stored 1 in terms of HRS of R1 and QB held 0 in terms of LRS of R2. To begin the write 0 operation at storage node Q, WBLB pulls up to 1 and WBL pull down to 0, and WWL pulled to 1, which turns on M1 and M2, as shown in Figure 4(a). Now a path has been formed between WBL to storage node Q, which forces R1 to switch their resistance state from HRS to LRS and write 0 at node Q, similarly reverse operation performed at

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Volume 9, Issue 1, Jan 2022

the storage node QB as shown in Figure 4(b). At this moment, R1 at LRS and R2 at HRS and make M3 turned on, and M4 turned off and writing 0 to node Q and 1 to node QB has been performed, After that the WWL signal reset to 0, which turned off M1 and M2 as shown in Figure 4(c).

Figure 5 shows the timing waveform of the write operation performed in 7T2M NvSRAM. At the end of the write operation, R1 is LRS. Through R1, there is a short circuit path from the power supply to the ground which contributes larger power to save this power. The EN signal is used in 7T2M NvSRAM, which drives to GND after write operation to cut the path from VDD to GND.

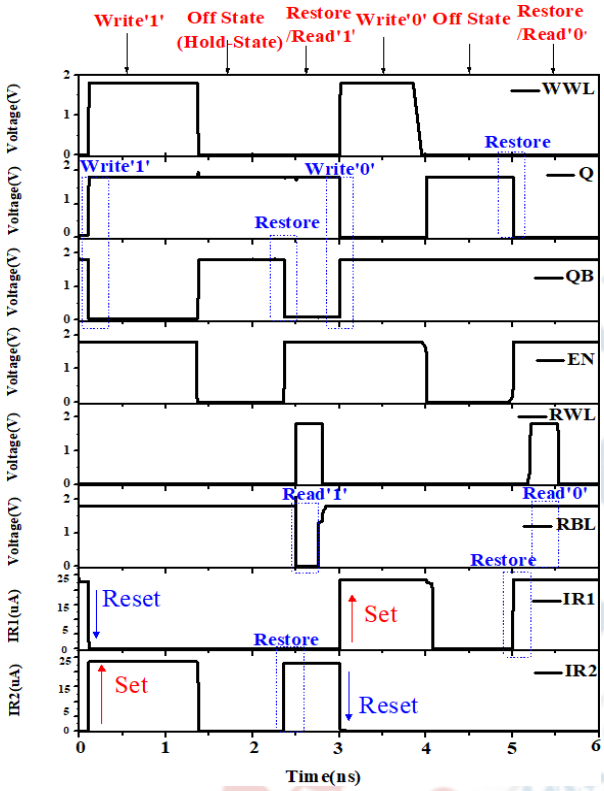


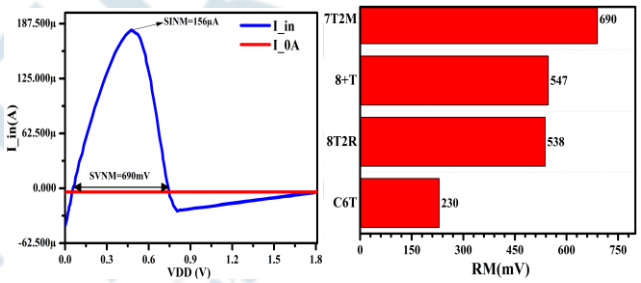
Figure 5: Timing waveform of 7T2M NvSRAM array for write, store/off state and self-restore/read operation.

B. Restore/Read Operation

To store the data non-volatility, the complimentary latched data can be stored onto the memristor by a self-inhibit mechanism [14] inherit in this cell. When data is successfully stored in the memristor, the EN signal drives to GND which cut the path from VDD to GND for the permanent data store in term of the resistance state of the memristor. To access the store data, EN signal drive from GND to VDD then non-volatile store data restore to Q and QB node automatically as shown in Figure 5 and can be accessed through M6 transistor for a read operation. During the read '1' operation, storage nodes Q at '1' and QB restore to '0', which turned on M6. When the value at RWL switch from '0' to '1', then transistor M5 change their state from off to on, and a path from RBL to VGND becomes transparent, and at same time VGND drives from '1' to '0'. When this path becomes transparent, the precharged RBL begins to discharge through this path and read '1' operation completed. After completion of a read operation, RWL pulled down to '0' RBL precharged to VDD as shown in Figure 5, while VGND drive to VDD to reduce the leakage current in read path during off.

IV. ANALYSIS OF 7T2M NVSRAM BIT-CELL

The benchmarks circuits of C6T, 8T,8+T [9], 8T2R [15], and the proposed 7T2M NvSRAM are implement with same 180nm SCL CMOS technology and TEAM memristor model [16] using cadence tool for the comparative analysis. This section presents the analysis of the proposed 7T2M NvSRAM bit-cell in terms of static and dynamic noise margin, leakage power, read/write access time, energy, and cell area, and compared with benchmarks circuit.



(a) (b)

Figure 6: (a) N-curve for RM calculation (b) Read margin comparison of various SRAM cells at VDD=1.8V.

A. Stability Analysis

Robustness of the memory cell is defined by its stability analysis. The proposed 7T2M NvSRAM is non-volatile in nature. Therefore, 7T2M NvSRAM cell does not need to hold voltage to maintain the cell during standby conditions. Hence, the read, write, and dynamic stability analysis is only concentrated in this paper.

1) Read Stability:

The N-curve [17] is used to compute the read margin (RM) of the proposed 7T2M NvSRAM cell by calculating the static voltage noise margin (SVNM) and static current noise margin (SINM), as shown in Figure 6(a). The SVNM is defined by the amount of DC noise that can be tolerated at node QB, and SINM is determined by the maximum DC that can be injected in the cell node without affecting the stored data. The read-decouple path is used in proposed 7T2M NvSRAM cell. Hence, a disturb-free read operation increase RM. Therefore, The RM of the proposed bit-cell achieves 1.69×, 13.16%, and 15.24% improvement over C6T SRAM, 8 +T [9] and 8T2R NvSRAM [15], respectively as shown in Figure 6(b).

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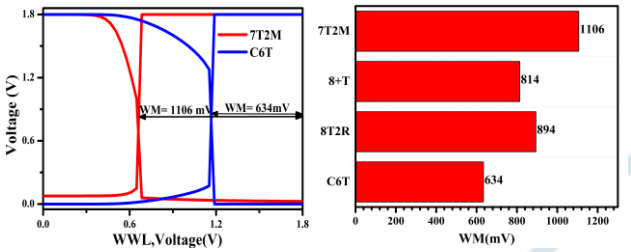
Volume 9, Issue 1, Jan 2022

2) Write stability:

The noise can be sustained at any SRAM cell node, including storage node, write word line, and read word line, which makes the essential investigation on all types of write margin definition [18]. Where sweep the WWL at both nodes to replicate real write operation, where both switch transistors (M1-M2) drive by WWL pulse. The write margin is calculated by subtracting WWL voltage with VDD when Q and QB node flip, as shown in Figure 7(a). The WM of the proposed cell is improved because of the memristor device with a high resistance ratio and threshold current. Therefore, The WM of the proposed 7T2M NvSRAM cell achieves 74%, 35.87% and 23.7% improvement over C6T, 8 +T SRAM [9] and 8T2R NvSRAM [15] cell, respectively as shown in Figure 7(b).



(a) (b)

Figure 7: (a) WM calculation of proposed 7T2M NvSRAM. (b) WSNM comparison of various bit-cells at VDD =1.8V.

B. Standby Power and Ion/Ioff ratio

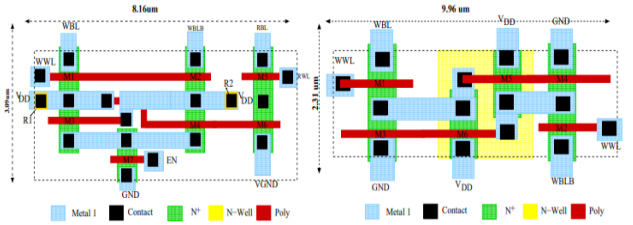
The standby power and Ion/Ioff ratio of bit-cell is one of the important factors for designing memory array since the total number of bit-cell in a row is limited by Ion/Ioff ratio, where Ion and Ioff are on and hold current of read path, respectively. The stacking transistor M7 is used in 7T2M NvSRAM to reduce the standby power. Therefore, The standby power of the proposed 7T2M NvSRAM is improved by 64.20%, 62.30%, 58.82%, over 6T SRAM, 8 +T SRAM, 8T2R NvSRAM, respectively, as observed from Table II. The VGND line in read path of the proposed 7T2M NvSRAM cell achieves 102%, 87.7% and 102.25% improvement of Ion/Ioff ratio over C6T SRAM, 8 +T SRAM [9] and 8T2R NvSRAM [15] cell, respectively.

Table II: Performance Analysis of various bit-cells

Parameters	7T2M NvSRAM	C6T	8T2R [15]	8+T [9]
Non-volatility	Y	N	Y	N
Write Delay (ps)	108	81	82	90
Read Delay (ps)	22	20 0	20	23
Read Energy (aJ)	16.89	17.8	18.9	19.20
Write Energy (fJ)	0.908	1.005	1.114	1.256
Store Energy(fJ)	0.596	NA	0.836	NA
Restore Energy(fJ)	0.296	NA	0.517	NA
Standby Power(pw)	5.13	14.33	12.46	13.61
I on/I off(10^6)	57.03	28.17	28.27	30.38

D. Cell Area

The layout of all SRAM cells is constructed using 180nm SCL technology in the Cadence Virtuoso Layout-XL tool to calculate the cell dimension of bit cells. Figure 8 shows a thin cell layout of 7T2M NvSRAM, and C6T SRAM cells. Table III shows the number of transistors and memristors required for designing each cell and the corresponding area of each SRAM. Due to use of memristor device in place of PMOS transistor, the area overhead of the proposed 7T2M NvSRAM is improved by 24% when compared to C8T. The extra transistor M7 for stacking effect is used to reduce leakage power therefore the area overhead of proposed 7T2M NvSRAM is increased by only 6% when compared to C6T.



(a) (b)

Figure 8: Thin cell Layout of (a) 7T2M NvSRAM. (b)C6T

Table III: Area overhead analysis of various bit-cells.

SRAM	NMOS	PMOS	Memristor	Area
7T2M NvSRAM	**7**	**0**	**2**	$24.56\mu m^2$
C6T	4	2	0	$23.00\mu m^2$
C8T	6	2	0	$29.6\mu m^2$

E. Performance Analysis

The performance analysis of 7T2M NvSRAM, C6T, 8 +T SRAM [9], and 8T2R NvSRAM [15] bit-cell are reported in Table II. In a write operation, the proposed 7T2M NvSRAM cell does not show improvement in write delay because of a memristor device, which required a larger time for switching the resistance state from LRS to HRS for writing logic '1' in terms of high resistance state. The memristor is a nanometer device, which consumes lower power compared to a CMOS device. Therefore, The write energy consumption of the proposed cell has improved by 9.6%, 18.14% and 27.17% compared to C6T SRAM, 8T2R NvSRAM [15] and 8 +T SRAM [9] cells, respectively. The write delay of the proposed bit-cell can be improved by decreasing the HRS ratio to LRS [19], but this will increase the power dissipation during the write operation. Due to self-inhibit data storing mechanism, the store and restore energy consumption of the proposed cell is improved by consume 28.7% and 50.1% when compared to 8T2R NvSRAM [15] as observed from Table II. In read operation the proposed 7T2M NvSRAM cell consume 5.1%, 10.63% and 12.03% lower read energy compared to C6T, 8T2R NvSRAM [15] and 8 +T SRAM [9] cells.

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International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

Volume 9, Issue 1, Jan 2022

V. 7T2M NVSRAM BASED IN-MEMORY COMPUTATION

The IMC [2] means that data computing, data transfer, and data storage are executed inside the memory array. The basic concept behind NvSRAM-IMC is to enable multiple read word lines (RWL) simultaneously in the 7T2M NvSRAM array, which makes common RBL for enabled multiple 7T2M NvSRAM bit-cell. We can directly compute the Boolean operation of stored operands in multiple 7T2M NvSRAM bit cell through sensing the common RBL at sense amplifier. The single column of 7T2M NvSRAM array with write driver, VGND driver, sensing circuit, and the control signal is used for write, restore/read, and IMBC operation as shown in Figure 9.

Table IV: Performance comparison of IMBC based on various bit-cells

Bit-cell	IMBC Operation	Avg. Energy/bit(fj)	Latency
C6T	NAND,NOR	7.31	3
4+2T [8]	NAND,AND NOR,OR,XOR	6.39	3
8+T [9]	NAND,AND NOR,OR,XOR	19.30	1
8T [9]	NAND,AND NOR,OR,XOR	10.81	3
7T2R	NAND,AND NOR,OR,XOR	4.29	1

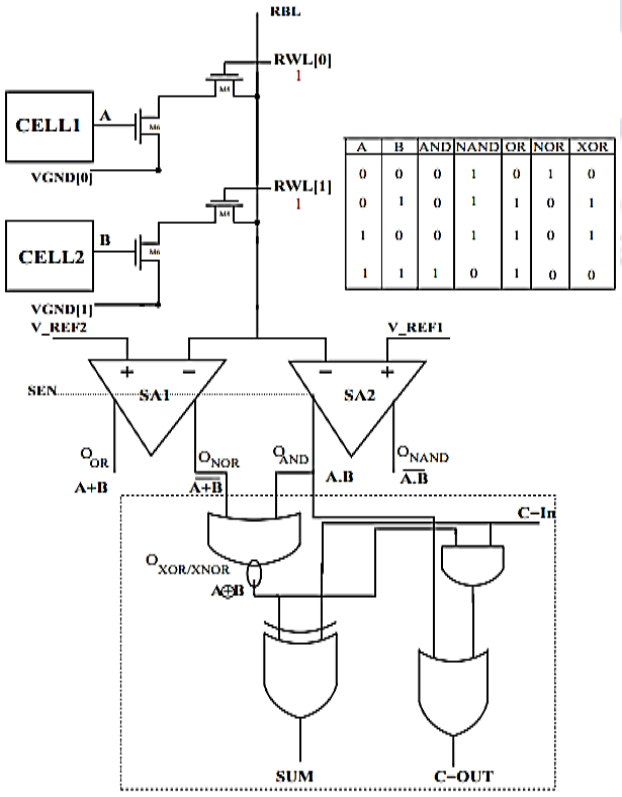

Figure 9: The schematic of circuit for performing IMBC operation.

A. IMBC in 7T2M NvSRAM

Figure 9 shows the IMBC operation of NAND, AND, NOR, OR, XOR Boolean logic using 7T2M NvSRAM based IMC. The RBL is connected to the SA1 and SA2, and VREF 1 and VREF 2 are connected to SA1 and SA2, respectively, to perform all IMBC operations in a single cycle as shown in Figure 12(c). The reference voltage VREF 2 and VREF 1 are used to compare the RBL voltage by using SA2 and SA1, respectively. To produce correct IMBC operation result, the idle VREF 1 is set to 0.9V and idle VREF 2 is set to 1.6V when VDD=1.8V. The signal WWL is kept at low, SEN signal is kept at high, and RWL signal is kept at high. The voltage on RBL (denoted as VRBL) is initially precharged to VDD. A sensing scheme is used to distinguish the different values of VRBL and thereby compute all logic operations on store operand in bit-cell in a single read cycle, which is proposed in [20]. The RWL[0] and RWL[1] are enabled to perform the IMBC operations (NAND, AND, OR, NOR, XOR) on operands A and B. The resulting voltage at RBL (VRBL) depends on the operand value store in the bit-cell [21], [22]. The resulting voltage of RBL is compared to VREF 1 by using SA2. NAND and AND operation on operand A and B are obtained at the output O1 and O2 of SA2, respectively. The resulting voltage of RBL is compared to VREF 2 by using SA1. NOR and OR operation on operand A and B is obtained at the output O1 and O2 of SA1, respectively.

B. Near Memory Arithmetic Operation in 7T2M NvSRAM

IMC in 7T2M NvSRAM provides In-Memory Boolean logic computation in a single cycle. A single bit full adder can be realized using an extra peripheral circuit and XOR output, as shown in Figure 9. The adder's performance can be improved using the approach reported in [22], where the n-bit adder can be implemented in the N-cycle. The multiplication operation can be performed with the help of the addition operation. The division and subtraction can be implemented with the support of XOR observed at the output

VI. ANALYSIS OF 7T2M NVSRAM-IMC

This section presents the analysis of 7T2M NvSRAM IMC in terms of energy per bit operation and the number of read cycles required to execute all IMBC operations. The IMC architecture is implemented with the help of the 7T2M NvSRAM bit-cell. The IMBC operation of NOR, OR, NAND, AND, and XOR is demonstrated. The average energy consumption per bit operation is presented in Table IV. The latency shown in Table IV presents the total no. of memory cycles required for performing all logic operations. IMC architecture based on the proposed cell has 25.44%, 14.71%, 49.58% and 71.76%, reduction in average energy consumption for per bit operation over IMC architecture based on [5], [8], [9] and [9], respectively. The IMC ability of the proposed 7T2M NvSRAM cell shows that it can be

efficiently used as ALU and memory in the computing system. It has a broader application in the computation system. One of the utilization is a standard Von Neumann General purpose processor with the SRAM-based register file replaced by a 7T2M NvSRAM array that can provide high performance and increased energy efficiency. Another application is a low-power accelerator in artificial intelligence and a machine learning processor.

VII. CONCLUSION

In this paper, 7T2M NvSRAM Bit-cell with an enhanced read/write noise margin is proposed for energy-efficient IMBC. The area overhead of the proposed 7T2M NvSRAM is reduced when compared to C8T SRAM due to the nanometer memristor device and NMOS transistor only. The read decouples path with VGND line and high resistance ratio of the proposed 7T2M NvSRAM improve 2.46× in RM and 5.32% in read energy when compared to C6T SRAM. The write mechanism of the proposed 7T2M NvSRAM improves 23.71% in WM over recently reported 8T2R NvSRAM. The V VSS with stacking transistor is improved 2.79× in standby power at the cost of the extra transistor over C6T. The proposed 7T2M NvSRAM can also perform In-memory Boolean computation with memory storage due to the read decouple path. The proposed 7T2M NvSRAM bit-cell demonstrates computation feasibility with the SRAM memory array by implementing In-memory Boolean computations in the SRAM array. The proposed 7T2M NvSRAM improved 25.44%, 49.58%, and 14.71% in average energy per bit IMBC operations over C6T, C8T, and 4+2T SRAM, respectively, which show that 7T2M NvSRAM can be a potential candidate for developing low power embedded memory chips for IMC based Internet of things (IoT).

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