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Displaying Image through VGA Cable using Verilog

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***Abstract*--- VGA (Video Graphics Array) is a standard display interface that has been widely used. This paper represents the design and implementation of VGA controller by displaying some prestored images into the FPGA memory. Detailed information is focused on the system architecture and software programming. This controller is developed using Verilog HDL and VHDL (hardware description language). The system can display various types of images or patterns. Verilog HDL is used to describe and program the gates and counters in FPGA blocks in order to construct desired logic circuit in it. The main purpose of this project is to design and implement VGA Controller on FPGA and to display an image on VGA display by storing it in memory. Therefore, the block diagram for VGA Controller is designed and the VGA Controller program is written based on the block diagram using VHDL and Verilog. All the basic functions that are required to run the code of VGA controller is written in the Verilog code and testbench of that following functions is also created to ensure the proper functioning of VGA controller without any errors. Finally, the completed program is implemented on FPGAs chip of SPARTAN-3E Development and Educational Board and successfully able to display image.**

I. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are digital ICs (Integrated Circuits) that permit us to program a customized Digital Logic as per his/her requirements. The term "Field Programmable" implies that the digital logic of the IC isn't fixed during manufacturing and that we can modify(program) per our needs. so as to produce functionality, an FPGA consists of Configurable (or Programmable) Logic Blocks and configurable interconnects between these blocks.[1] VGA (video graphics array) could be a display screen standard. It's an easy process to attach a system with a monitor for showing information that carry images, videos, different patterns. VGA may be a standard display interface that has been widely used is shown in figure 1. There's the necessity of displaying the results of any process in real time so VGA is that the basic standard which might be used. Modern VGA displays support multiple display resolutions, and therefore the VGA controller defines the resolution by producing timing signals to manage the assorted patterns. The monitor screen for a typical VGA format contains 640 columns by 480 rows of picture elements called pixel. All the timing signals are predefined in keeping with the mentioned resolution, using 25Mhz pixel clock and 60 Hz refresh rate, the pixel and contours are conclude. The VGA controller contains two counters.[2] One counter increment on pixel clocks and controls the timing of the h_ sync (horizontal sync) signal. The counters are setup in such the way that display time starts at counter value 0, and therefore the counter value = pixel‟s column coordinate. The horizontal display time is followed by a blanking time, which has a horizontal porch, the horizontal sync pulse itself, and also the horizontal porch, each of specified duration. At the tip of the row, the counter resets to begin the subsequent row. the opposite counter increments as scanning of every row completes, therefore controlling the timing of the v_ sync (vertical sync) signal.[3] Again, the above mentioned process is repeated just in case of vertical sync, during this case the counter value = pixel‟s row coordinate during the display time. And rather like horizontal display time before, the vertical display time is additionally followed by a blanking time, with its corresponding porch, sync pulse, and porch. Once the vertical blanking time completes, the counter resets to start the following screen refresh. Figure 3 illustrates the blanking time of horizontal and vertical display time. the most purpose of this project is to display in image on VGA screen by designing a VGA controller. To display a picture on VGA display first of all the RGB data of image is extracted in RGB format then arrange that data in CSV file or excel file. The arranged data is then loaded within the FPGA memory. Once all this is often done the following step is to write down VGA controller code using Model Sim or Xilinx ISE which is able to compile, run and simulate the written program and eventually display that on VGA screen[1-5].

Spartan 3E Development and Education Board

The Spartan-3E Board provides a powerful and highly advanced self-contained development platform for designs

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targeting the Spartan-3E FPGA from Xilinx. The Spartan3e Development board is also a circuit design and implementation platform[6-7]. It's suitable for an honest range of exercises in courses on digital logic and computer organization, from simple tasks that illustrate fundamental concepts to advanced designs. It consists of on board lcd, light controller, VGA, RS232, UART, keypads, and relay to create a standalone versatile test board. Below is that the image of spartan 3e development board.[4]

VGA Controller

Monitor screens of a VGA monitor comprise 640 columns in it and 480 rows are available for the picture element which is also known as a pixel. A combination of multiple pixels creates an Image. To display an image we have to turn on & off the particular pixels. Monitor scans the entire screen continuously.[5] The Process of scanning the entire screen starts from row "0", Column „0" in the top left corner of the screen and it continuously moves towards the right until it reaches the last columns. When this process reaches the end of a row it moves back to the beginning of the next row. When it reaches the last pixel in the bottom right corner of the screen. It Moves back to the top left corner and repeats the scanning process. Figure 2 and 3 shows the clear explanation of scanning process. In Way to reduce blinking on the screen, the whole screen must be scanned 60 times per second. This duration is known as refresh rate. If the refresh rate is less than 30Hz then this blinking can be detected by the human eye. To reduce this blinking from the interference refresh rate more than 60Hz is used. When the horizontal and the vertical retraces all the pixels are turned off[8-11].

The VGA monitor is controlled by five types of signals which are mentioned below:-

1. Red
2. Green
3. Blue
4. Horizontal Synchronization
5. Vertical Synchronization

Red, Green, and blue that represents the color, collectively also known as RGB signal. This RGB signal controls the color of the pixel at a particular location on the screen. Which are analog signals with the range of 0.7 volts to 1.0 volt. The various colors are obtained by the increment or decrement in the voltage depending on how many bits we need for individual RGB colors as higher the bits we take more the of these RGB signals are also known as digital signals which means there will be any two outputs either on or off.[6] And the rest of the two horizontal and vertical signals are used to control the time of scanning rates. Horizontal synchronization is used to control horizontal deflection in the VGA monitor. Whereas vertical Synchronization is used to control vertical deflection in the VGA monitor. The horizontal synchronization signal determines the total time taken to scan a row and the Vertical Synchronization signal determines the total time taken to scan the whole screen. By operating these five signals images are displayed on the screen. To get the resolution of 640X480 we need a clock with the frequency of 25.175MHZ. For clock Frequency 25.175MHz the time duration is mentioned in the next section of VGA Signal timing and whose diagram is shown in Figure 4. By default 50Mhz clock is present on the spartan 3E board and we have converted that clock to 25Mhz by using frequency divison and in some FPGAs DCM(digital clock manager) is present which solves a variety of common clocking issues. The block diagram shown in figure 1 will be showing the internal connection that how actually the image is stored and then same image is fetched using memory address location of that particular image. In the output we get only five signals from vga controller through which we can display an image on VGA screen.[7]

Design Flow of VGA Synchronization

Primarily, the reset button is checked. While checking the reset button there is two possibility either it will reset to 0 or 1. If reset button is 1, "h_count" and "v_count" will be reset to 0. If reset is equal to 0, it will further check the value of "h_count". If the "h_count is not equal to 799 than "h_count" is incremented by 1. When the value of h_count is equals to 799 one horizontal scan completes and the counter will be reset to 0. After checking the value of "h_count", it will check the value of "v_count" which is equal to 520 or not. If the "v_count" is not equal to 520, "v_count" will be increased by 1 and once the value of "v_count" is reached to 520, it will be reset to 0. This is because of one complete vertical scan which is begin from 0 to 520. Now we are going to mention about "h_count" when it is incremented by 1. It will check whether the value of "h_count" is less than 96 or not. If the value of "h_count" is less than 96, "display" will be set to 0. The value of "display" will be stored into "h_sync". "THE VALUE OF "H_COUNT" IS LESS THAN 96 INDICATED HORIZONTAL RETRACE". Else, "h_display" will be set to 1 and then stored into "h_sync". It will also check whether the value of "h_count" is lesser than 784 and greater or equal to 144 or not. The value of "h_count" is lesser than 784 and greater than 144. This value will indicate the display area for the horizontal scan. Now we will discuss about the "v_count" is increased by 1. it will check whether the value of "v_count" is less than 2 or not.If the value of "v_count" is less than 2, "V_display" will be set to 0 and the value of "V_display" will be stored into "v_sync". Else, "V_display" will be set to 1 and then stored into "v_sync". "VERTICAL RETRACE IS DEFINED BY THE VALUE OF

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"V_COUNT" LESS THAN 2". It will also check whether the value of "v_count" is greater or equal to 34 and lesser than 514 or not. The value of "v_count" lesser than 514 and greater or equal to 34 indicates the display area for vertical scan. The value of "h_sync" and "v_sync" are used to multiply together and the Output value is stored in the "Display_EN". And then, the value in "Display_EN" is once more keep into "video_on". And finally, the resultant signal which combines of vertical and horizontal scan will consist of the information which is need to display on the VGA screen to show the final output[12].

VGA Signal Timing

VGA control timing is shown in table below. The table shows the relation between each of the timing symbols[13]. Based on the observation from various VGA displays the timing is shown in the below table of sync pulse width (TPW), front porch and back porch intervals (TFP and TBP). These intervals do not carry any information. The signal timings in Table 1 below are derived for a 640-pixel by 480-row display using a 25 MHz pixel clock and 60 Hz ±1 refresh.

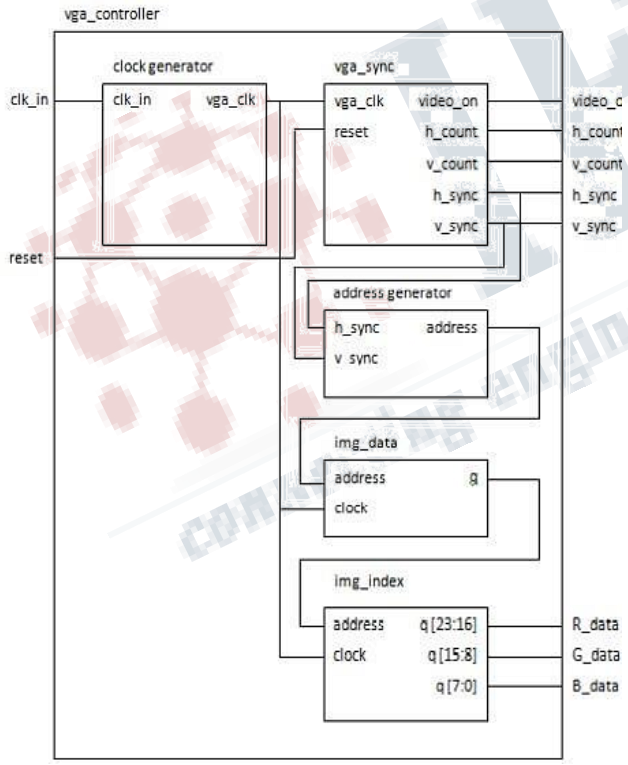

Figure 1: Block diagram of VGA controller

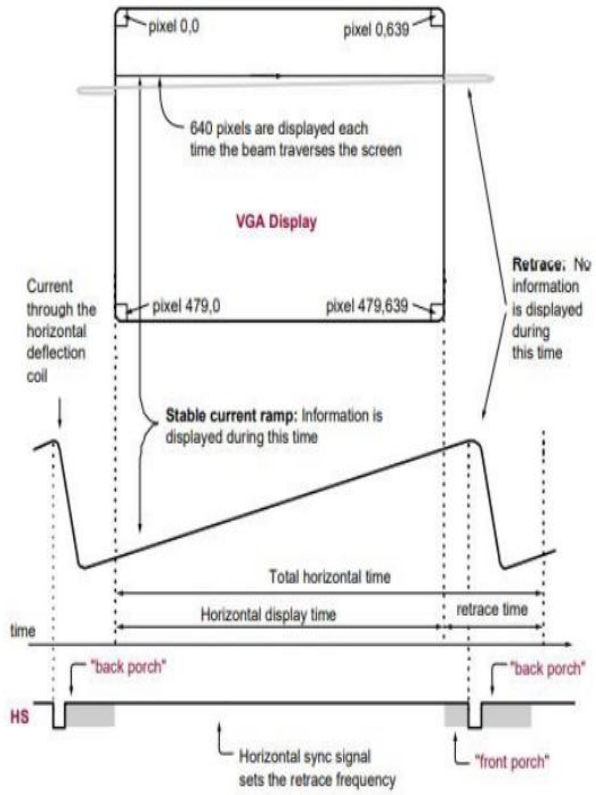

Figure 2: Scanning pattern of VGA and Vertical Synchronization

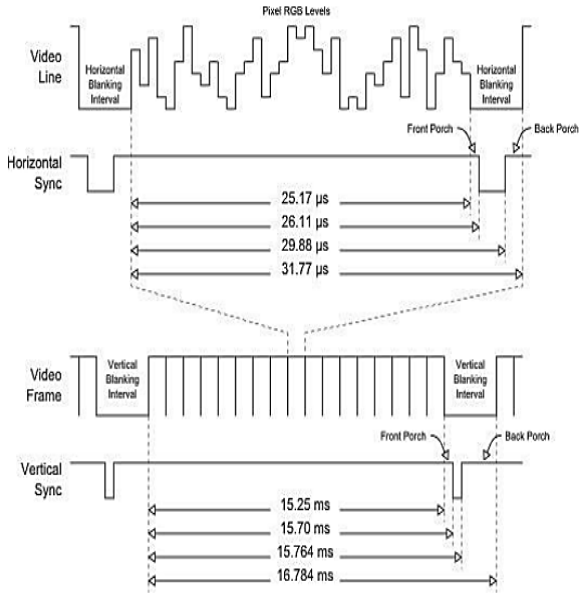

Figure 3: Horizontal timing diagram

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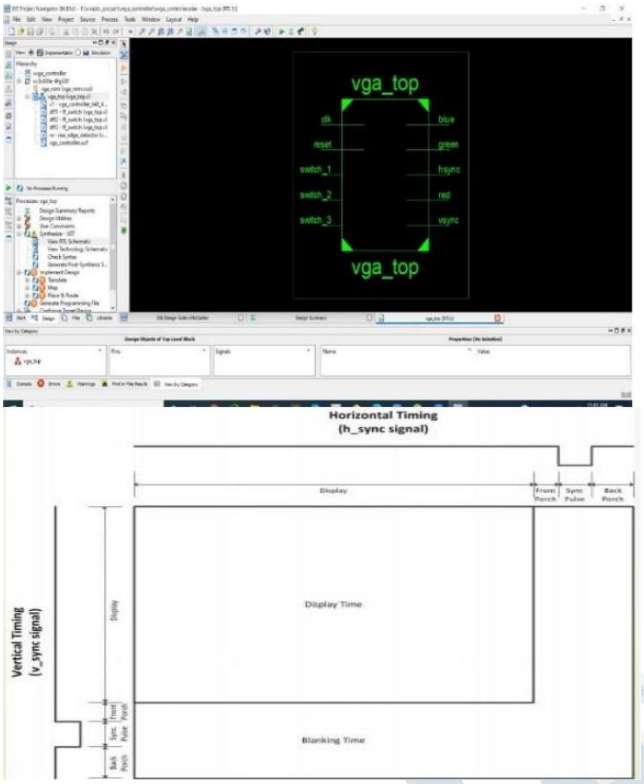

Figure 4: Top Module of VGA simulation timing

TABLE 1 – VGA CONTROL TIMING

Symbol	Parameter	Vertical Sync			Horizontal Sync	
		Time	Clocks	Lines	Time	Clocks
T_S	Sync pulse time	16.7 ms	416,800	521	32 µs	800
T_{DISP}	Display time	15.36 ms	384,000	480	25.6 µs	640
T_{PW}	Pulse width	64 µs	1,600	2	3.84 µs	96
T_{FP}	Front porch	320 µs	8,000	10	640 ns	16
T_{BP}	Back porch	928 µs	23,200	29	1.92 µs	48

II. CONCLUSION

In this project, a prototype of VGA controller is made using SPARTAN 3E development and education board, the code is written in VERILOG and VHDL using the software MODELSIM and XILINX ISE and the bit file was created using Xilinx ISE and finally it burnt into board. Result was verified by checking the various pattern of RGB on the display screen and a prestored image. Problems encountered during the whole process was that some code was not synthesizable that was resolved by modifying the process of coding and making it synthesizable. FPGAs are best to be used as VGA controller as we have to just write few behavioral models. We can even simulate it with test benches and can see waveform of VGA control timing.

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