ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 5, May 2018

Timing Optimization In Engineering Change Order Stage For Functional Unit Blocks In Soc Design

[1] Asha Y N, [2] Dr.Shilpa D R, [3] Arun Seetharaman
[1] PG Student, VLSI Design & Embedded systems, R. V. College Engineering, Bangalore
[2] Associate Professor, R. V. College Engineering, Bangalore, India
[3] Digital Design Engineer, Intel technologies India Pvt.ltd, Bangalore, India

Abstract- **Engineering Change Order (ECO) is important in correcting the late-found errors that arise commonly in designing sequential circuits. As the number of corners and number of modes increases, the possibility of setup and hold conflict raises. Hold times violations are critical as they lead to permanent failures in the design. A hold time ECO flow is proposed in the paper to fix negative min path violations. It uses buffer insertion and cell replacing as the main techniques to increase the delay of the path so as to make the margin more positive. The proposed methodology increases the time margin by 74.77% .The total negative slack and worst negative slack got improved by 91.68% and 87.01% respectively. It is found that 63.87% hold violated paths can be fixed using the proposed methodology.**

Index Terms— **Setup time, hold time, Engineering change order, negative paths, skew, timing margin, Total Negative Slack(TNS), Worst Negative Slack(WNS).**

I. INTRODUCTION

To accommodate more late design changes, the increasing hardware system complexity makes engineering change order (ECO) important. The increasing time-to-market pressure, makes more and more design errors and deficiencies to be found in late design cycles. Synthesizing a whole new design takes much effort of the design engineer, so it is crucial to rectify the deficient design with minimal perturbations for the design process to meet its timing requirements. As a result, engineering change orders (ECOs) are widely applied to incrementally repair design violations and thus reduce the need to backtrack to earlier design stages for design correction. ECO problems can be divided into 3 categories based on the levels of abstractions and objectives. Functional ECO aims at rectifying the functionality of old implementations to meet new specifications at the logic level. Physical ECO is concerned with realizing the changes of the functionally rectified netlist at the physical design level. Timing ECO focuses on resolving timing violations of a circuit at the post-layout stage. Functional ECOs may be decomposed into: 1) a logic difference analysis stage; and 2) an implementation (rewiring with spare cells) stage, which are often resolved separately. Timing violations may result from the selection of spare cells with insufficient driving power or spare cells with unsatisfactory routing cost. So, functional ECO can be insufficient without the timing ECO. Hence, timing ECO is indispensable to fix timing violations due to unexpected delay sources in the original circuit and also due to functional ECO. This paper is mainly concerned with timing ECO, which aims at fixing the hold time violations that occur in later design stages.

1.1 Previous Works

Timing ECO, was considered in [1], and [3]. An optimization flow based on dynamic programming is proposed in [1] the work in the paper concentrates on achieving buffer insertion and gate sizing. By replacing a spare cell with cell with better driving power the Gate sizing was realized on a timing critical path through rewiring. By connecting a buffer-type spare cell on a timing critical path the buffer insertion was realized. In [3] a similar buffer insertion technique is utilized to resolve timing violation under output-loading and input slew constraints. Gate sizing is likely to succeed for some target gate mostly when there is a nearby spare cell with the same gate type and of proper size; buffer insertion is likely to succeed for some timing-critical path mostly when there is a nearby buffer-type spare cell of proper size. Hence, the optimization quality of these methods heavily relies on the availability of proper spare cells near the timing critical region. When the spare cells are inserted in a way favoring functional ECO [4], these approaches can be limited. To address this issue, a recent

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 5, May 2018

work proposed in [5] reconstructed critical sub circuits for timing fix.

1.2 Preliminaries

It is necessary to fix all hold time violations, as they lead to permanent failures during design time. Setup-time violations could be addressed by increasing the clock period. Therefore, it is important to find and fix all the hold-time violations so as to ensure the proper functioning of the circuit.

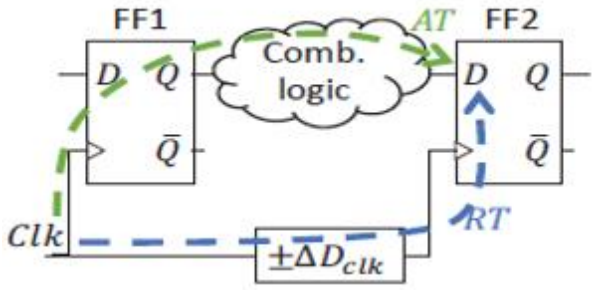

Figure1:flip-flop timing constraints

The hold time constraint can be defined as
actual arrival time AT = Dclk−q1 + Dcomb.,…… (1)
required arrival time RT = Dhold2 +ΔDclk,
hold slack S = AT − RT ≥ 0,

where Dhold2 is the hold-time of the second flip-flop, Dclk−q1 is the propagation delay of the first flip-flop (clock-to-q), ΔDclk is the clock skew, and Dcomb. is the delay of the combinational logic (depicted in Figure 1a). In an extreme case, where there is no combinational logic (e.g. shift register), the hold-slack depends on the hold-time and propagation delay of the flip-flops and the clock-skew. According to Equation (1), any increase in the required time (RT) or decrease in the arrival time (AT) reduces the hold slack, which might lead to a functional failure in the circuit. Therefore, an additional margin has to be considered to prevent such a failure (i.e. by increasing Dcomb). Since a single-corner nominal hold-time analysis is not able to capture the entire distribution of the variables, it cannot find all the hold-time violations.

1.3 Problem Formulation

The timing ECO problems can be defined as follows.
Problem : Given a placed and routed circuit netlist including a set of placed spare cells, a technology library, and required timing constraints, the objective of the timing ECO problem is to rewire the design such that all the timing requirements are met without affecting the functionality of the circuit.

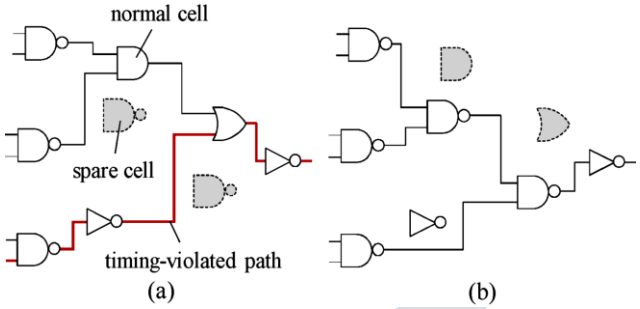

Figure 2. (a)Example Circuit with timing violation. (b) Circuit rewired for timing improvement.[5]

Figure 2 shows an example of timing ECO. A circuit with timing violation is illustrated in Fig. 2(a). It can be rewired to improve timing as shown in Fig. 2(b). Note that the timing optimized circuit is functionally equivalent to the original one.

II. METHODOLOGY

As feature size continues to scale down aggressively in VLSI fabrication, cross talk, buffering and process variations becomes critical in achieving timing closure. Timing analysis and optimization techniques needs to consider each of these parameters and their interactions. In this section we are going to propose a hold time ECO flow, which aims at fixing the hold violations that comes at later stages of design. The proposed flow is as shown in figure 3. To ensure correct data synchronization, hold time fixing is necessary. It serves as the final step of timing closure for IC design. Unlike setup time violations which are resolved by reducing the frequency, hold time violations are fatal. As the physical design flow progresses, the timing information becomes more accurate. So, the repair performed at early stages is insufficient at later stages. Therefore, fixing hold time violations using free space, without compromising the circuit performance is more challenging. There are many methods to fix hold time violations that occur in synthesis flow. The most popular method is to insert buffer. By inserting the buffer the delay increases across the path, hence the time margin becomes more and more positive. Time margin here is the difference between the required window and the valid window. Required window comprises of required setup and hold time requirements and the valid window consists of the actual timing parameters. As the time margin becomes more positive, there will be enough hold time available for the data to become stable, hence the hold time violation can be resolved.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 5, May 2018

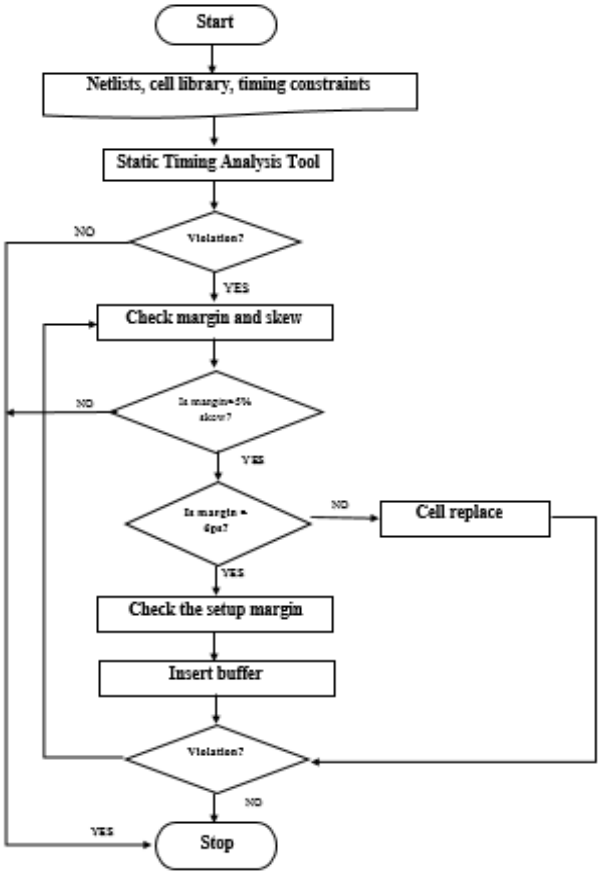

Figure 3: Proposed Hold time ECO flow

2.1 ALGORITHM:

The proposed algorithm for fixing min path violations ie, hold violations is as follows.

- Give the netlists, timing constraints and cell library as the input to the Static timing analysis tool.
- Check if there are any negative internal min paths ,if yes those paths needs to be fixed
- Check margin and skew of the violated paths, if margin>5% skew, on those paths buffer insertion or cell swapping can be applied
- Check the time margin, if time margin> 6 ps , insert buffer if setup margin is affordable, manually in the ICC interface
- If the margin is <6ps, swap the cells, ie , swap Low Threshold Voltage (LVT) cells with Standard Threshold Voltage (SVT) cells in the paths where Setup margin is affordable. As SVT cells add more delay into the path and hence the time margin increases.
- Re-run the STA tool, Check whether there are any violations still left.
- Repeat the same procedure until all paths get fixed.

III. RESULTS AND DISCUSSION:

The timing analysis is carried out for a functional unit block. Table 1 represents the timing paths which had negative margin that are leading to hold time violations in the circuit. It is observed that for path 5,7,8,9 and10 the margin is below 6ps, hence the cells can be replaced in those cases. But for the remaining cases the buffer is added in the path

Table 1: Paths before hold fixing

SL NO	PATH	PATH TYPE	MARGIN BEFORE	MARGIN AFTER
1	PATH 1	FF-D-FF	-0.012	0.0291
2	PATH 2	FF-D-FF	-0.01	0.0372
3	PATH 3	FF-D-FF	-0.007	0.0291
4	PATH 4	L-D-L	-0.007	0.0152
5	PATH 5	L-D-L	-0.004	0.0093
6	PATH 6	L-D-L	-0.006	0.0674
7	PATH 7	L-D-L	-0.003	0.0122
8	PATH 8	L-D-L	-0.003	0.0210
9	PATH 9	FF-D-FF	-0.002	0.0172
10	PATH 10	L-D-L	-0.002	0.0241

From table 1 it can be inferred that the timing margin got increased by 74.77% when the negative margin paths is fixed using proposed ECO flow. Fixing the negative min paths using the proposed flow will have effect on Total Negative Slack (TNS) and Worst Negative Slack of the circuit as shown in Table 3 and Table 4. Negative slack at any output indicates that the circuit doesn't meet timing. As the slack becomes more positive it is an indication that the circuit is meeting timing requirements.

Table 3: Before Hold ECO

SL NO	CIRCUIT	TNS	WNS	#Negative paths
1	Functional Unit Block 1	-0.121	-0.016	32
2	Functional Unit Block 2	-0.015	-0.004	9
3	Functional Unit Block 3	-0.231	-0.013	71

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 5, May 2018

Table 4: After Hold ECO

SL NO	CIRCUIT	TNS	WNS	#Negative paths
1	Functional Unit Block 1	-0.002	-0.001	6
2	Functional Unit Block 2	-0.002	-0.001	6
3	Functional Unit Block 3	-0.023	-0.001	31

From table 3&4, it is observed that the Total Negative slack and worst negative slack got improved by 91.68% and 87.01% respectively also we can see that the number of negative paths decreases as shown in Figure 4.

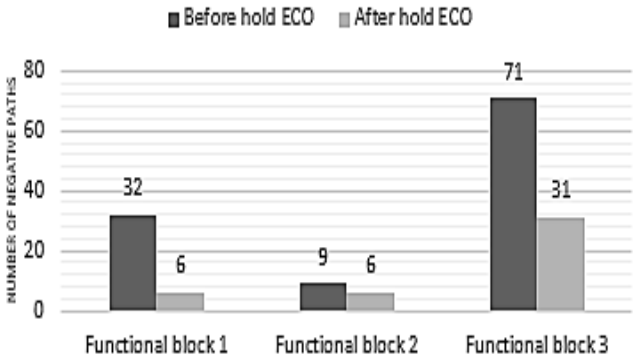

Figure 3: Number of negative paths before and after hold ECO

From Figure 3 it can be observed 63.87% of hold violating paths can be fixed using the proposed hold fixing methodology.

IV. CONCLUSION

A hold fix ECO flow is proposed in order to fix the hold time violations. The main techniques employed here is buffer insertion and cell swapping. Buffer insertion adds the delay to the negative timing path to make the timing margin more positive. In cell swapping we replace Low Threshold Voltage Cells by Standard Threshold Voltage Cells in order to increase the delay of the path. These two techniques, combined together will give effective results as the number of negative paths got reduced by 63.87%.Hence the proposed hold ECO flow proves to be efficient in fixing the hold time violations that occur in later design stages.

REFERENCES

[1] Y.-P. Chen, J.-W. Fang, and Y.-W. Chang, “ECO Timing Optimization using Spare Cells,” Proceedings of International Conference on Computer Aided Design, pp. 530–535, Nov. 2007

[2] Y. Kukimoto, R. K. Brayton, and P. Sawkar, “Delay-Optimal Technology Mapping by DAG Covering,” Proceedings of Design Automation Conference, pp. 348–351, June 1998.

[3] C.-P. Lu, M. C.-T. Chao, C.-H. Lo, and C.-W. Chang, “A MetalOnly-ECO Solver for Input-Slew and Output-Loading Violations,”Proceedings of International Symposium on Physical Design, pp. 191–198, Apr. 2009.

[4] .-P. Chen, J.-W. Fang, and Y.-W. Chang, “ECO Timing Optimization using Spare Cells,” Proceedings of International Conference on Computer Aided Design, pp. 530–535, Nov. 2007

[5] K. H. Ho, J. H. R. Jiang and Y. W. Chang, "TRECO: Dynamic Technology Remapping for Timing Engineering Change Orders," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 31, no. 11, pp. 1723-1733, Nov. 2012.

[6] Y.-M. Kuo, Y.-T. Chang, S.-C. Chang and M. Marek-Sadowska,“Spare Cells with Constant Insertion for Engineering Change,” IEEE
Transactions on Computer-Aided Design, vol. 28, no. 3, Mar. 2009

[7] D. Pandini, L. T. Pileggi, and A. J. Strojwas, “Understanding and Addressing the Impact of Wiring Congestion during Technology Mapping,” Proceedings of International Symposium on Physical Design,pp. 131–136, Apr. 2002.

[8] M. S. Golanbari, S. Kiamehr and M. B. Tahoori, "Hold-time violation analysis and fixing in near-threshold region," 2016 26th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Bremen, 2016, pp. 5