ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 8, August 2017

A comparative study of Excess Loop Delay Compensation Techniques in Continuous Time Delta- Sigma Modulators

[1] Aditi Singh ,[2] Kumaravel S
[1] Mtech student, VLSI DESIGN
[2] Associate Professor at School of Electronics Engineering
VIT University,Vellore-632014,TamilNadu,India

Abstract **- Continuous time ∑Δ Convertor is an highly power efficient modulator which has overcome the pipeline and Discrete time modulator as they require more number of high speed gain stages.Morever it is has an aliasing free Nquist band which is made available by oversampling and an on chip filter is also present.The input is resistive with no sampling so it is easier to drive the entire modulator with miniscule noise and an on- chip clock conditioner is used.There are several drawbacks associated with CTDSM like clock jitter and excess loop delay.In this paper different techniques to reduce Excess Loop Delay(ELD) in a continuous time delta sigma modulator is analysed and presented.**

Index Terms— Delta-Sigma; Oversampling ;Clock jitter; Excess Loop Delay(ELD);Continuous Time ∑Δ Modulator (CTDSM).

INTRODUCTION

THE NAME DELTA-SIGMA MODULATOR MEANS INTEGRATION OR SUMMING (THE SIGMA) IS OVER THE DIFFERENCE (THE DELTA).

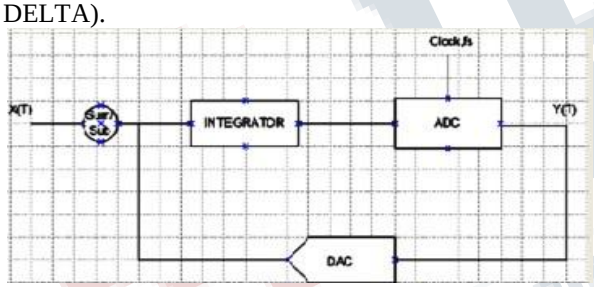

Fig 1.1 Basic Block Diagram of ∑Δ modulator

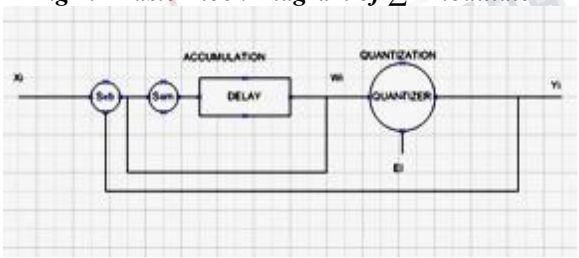

Fig 1.2 Sampled data equivalent structure of CTDSM

The integrator feeds the input signal to the quantizer then the quantized output is feeded back and subtracted from the input[1].

The average value of quantized signal tracks the input signal with the help of a feedback.The difference is stored in the accumulator which is self correcting. Thus,the integral components of CTDSM are a loop filter or loop transfer function,a clocked quantizer and a feedback DAC[2].

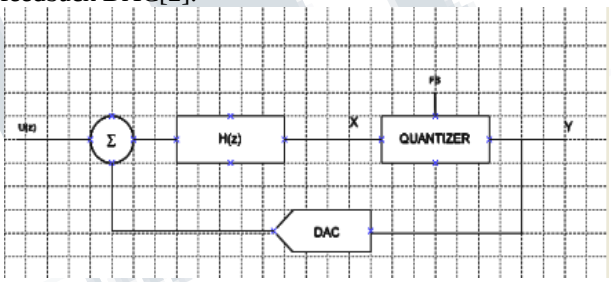

Fig 1.3 Simple Model of CTDSM

The presence of a nonlinear quantizer in a linear circuit makes the system behavior very complex to analyze.Thus the output consists of an signal transfer function associated with the input and an noise transfer function associated with the error signal.

∑Δ modulator are oversampling convertors where oversampling ratio is .The performance metrics linked with ∑Δ modulator are spectral leakage and uncertainity in periodogram, SNR, Dynamic range,Full scale amplitude,Maximum SNR,Maximum stable amplitude and Spurious free dynamic range.There are several nonidealities associated with CTDSM such as component mismatches and tolerance, multibit DAC level mismatch,inband noise,designing the first stage,clock jitter and excess loop delay.

Since Excess Loop Delay is the latest research topic so this problem is been taken as a motivation to write this literature. The research on this topic started since 1991 and is still ongoing. CTDSM are used in low frequency

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 8, August 2017

audio signals, the creation of black and white images for print from a gray scale input was another application where CTDSM noise- shaping techniques were used, also in application such as sensors,frequency synthesizers,digital radio,switched mode power supplies and motor controller.

II.EXCESS LOOP DELAY IN CONTINUOUS TIME DELTA SIGMA MODULATORS

The quantizer is an latched comparator whose output is driving the DAC.In an ideal case the current of DAC is responding with zero delay to the clock edge of the quantizer,while in practical use the transistor in the latch and DAC have non-zero switching times.So,there exists an delay in DAC current pulse and quantizer clock,called as Excess Loop Delay

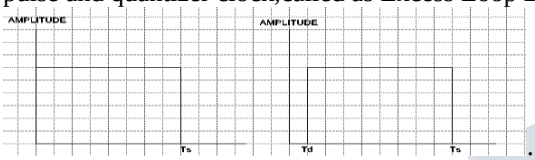

Fig2.1 Excess loop delay in NRZ DAC pulse.

III.CIRCUIT ANALYSIS ON VARIOUS TECHNIQUES FOR COMPENSATION OF EXCESS LOOP DELAY

ELD compensation in CTDSM has been dicussed in papers [3-7],The several methods used for compensation of ELD[3-7] has been analyzed in this section. I)(A) Since,ADC takes some time to make decision,So feedback DAC is clocked after some time delayed(ELD) from the sampling instant of the ADC. This Delay is responsible for the degradation of performance of loop.In this circuit a direct path is added [3] around the quantizer and with tuning of filter coefficients delay is compensated.

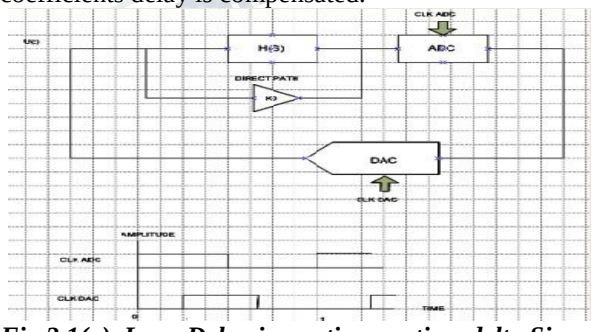

Fig 3.1(a) Loop Delay in continuous time delta Sigma Modulator

(B)

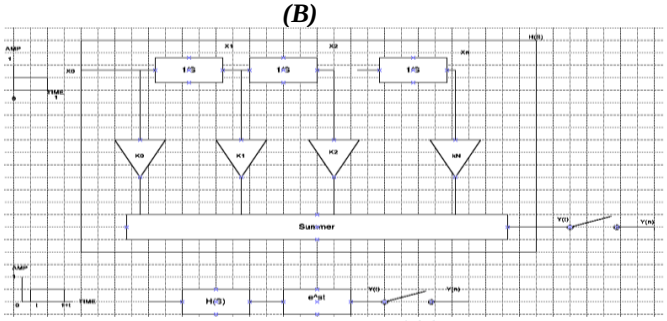

Fig3.1(b) Nth order NTF realization by a loop filter.

Here[3],Excess loop Delay is compensated by cascading a block in series.In this circuit operation two DAC pulse can be distinguished(NRZ and RZ).All the transfer function and modified transfer functions have been tabulated in the end of paper in Table I.

II)

In this Circuit dual slope based time interleave quantizer is used to compensate the ELD[4].The speed is increased by using multiple time interleaving quantizer,the overall latency with the delay contributed by other elements is added to the ELD.The speed limitation remains until ELD is not addressed.

In 3.2(a),a direct feedback path is added around the quantizer to realize a fast compensation path.In 3.2(b),the feedback loop is represented by sample and hold technique before quantizer,so delay is bypassed at degradation rate of SQNR.In 3.2(c),A digital differentiator is used to realize a fast compensation path before the quantizer to the input of the last integrator.In 3.2(d),two cycles of ELD compensation using a slow/fast path is realized.In 3.2(e),fast compensation path is realized by channel coupling.While one channel of TIQ is discharging,the time information of quantized signal sent to the other channel.

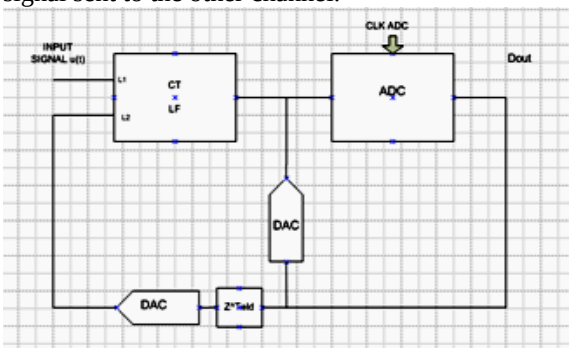

Fig 3.2 (a) Conventional method for Excess Delay

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 8, August 2017

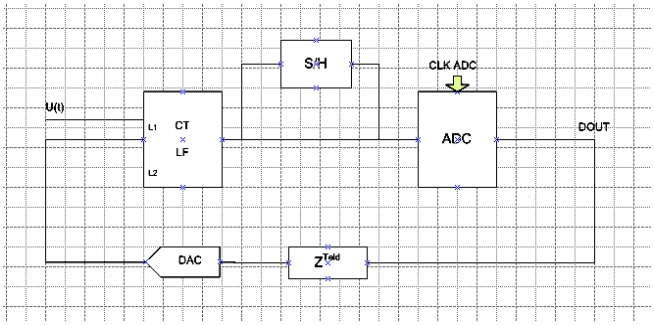

Fig 3.2 (b) Sample and Hold Circuitry used to bypass Excess Loop Delay.

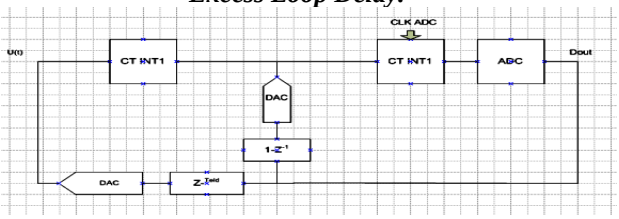

Fig 3.2 (c) A digital differentiator used to mitigate Excess Loop Delay.

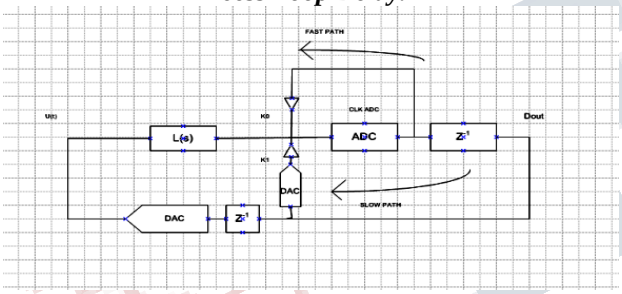

Fig 3.2(d) Fast and Slow path technique for Excess loop delay compensation having two cycles.

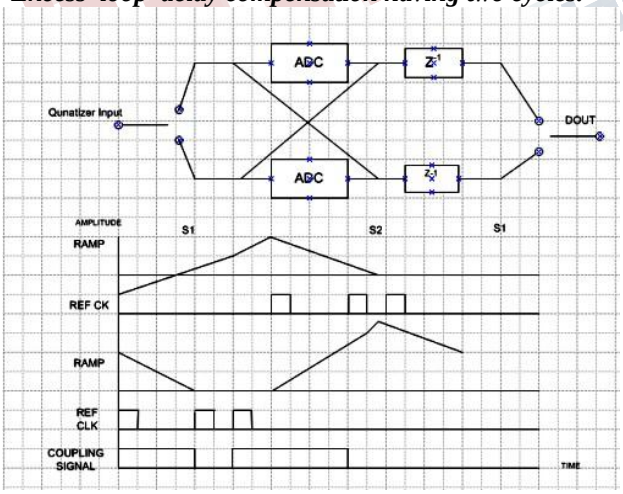

Fig 3.2(e) Channel coupling used for fast path compensation.

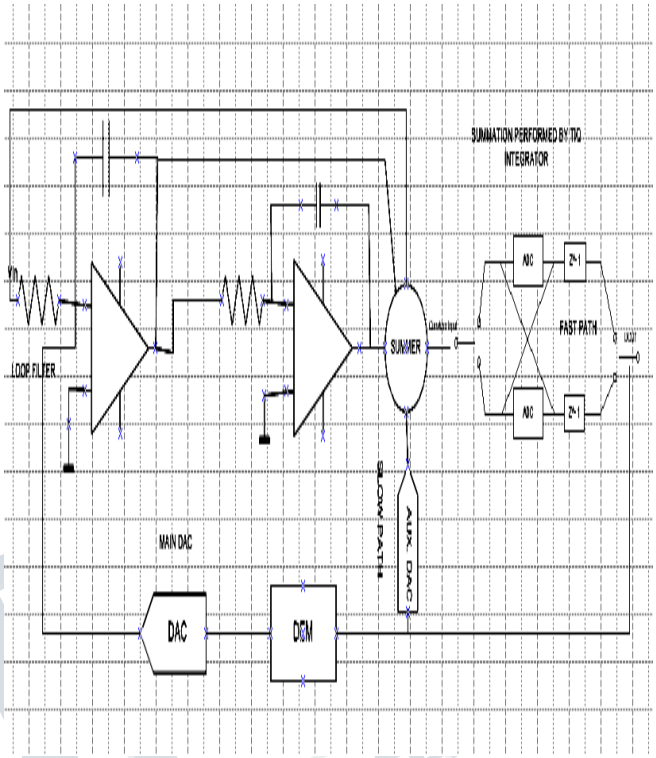

Fig 3.2 (f) Complete Design of Continuous time delta sigma modulator loop consisting of channel coupled Time Interleaved Quantizer.

The loop order is increased by the presence of Excess loop delay. This method is realized in figure 3.2(d) where Excess loop delay is compensated by the addition of K0 & K1,and the ideal NTFcan be restored[4]. Complete topology of the designed circuit as depicted in Fig3.2(f) consists of two satge of loop filter.Dual slope time interleaved quantizer is sampling the output of the loop filter.A summer is used before constructing a time interleave quantizer,but the summation of slow compensation path and feedforward path is done by integrators,in addition to the summation of dual slope and fast compensation path.

III)

A low noise Gyrator C topology is used[5] in order to achieve bandpass filter with high quality Factor which is used in 2nd order Delta Sigma Modulator.By the use of this technique the capacitor bank used in conventional CTDSM ∑Δ can be eliminated.This method makes CTDSM Delta Sigma Modulator usage flexible in digital recievers.With the usage of tunable

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 8, August 2017

Delta Sigma Modulator at intermediate frequency eliminates the selection of channel at radio frequency.The structure in fig 3.3(a) is flexible for low power.

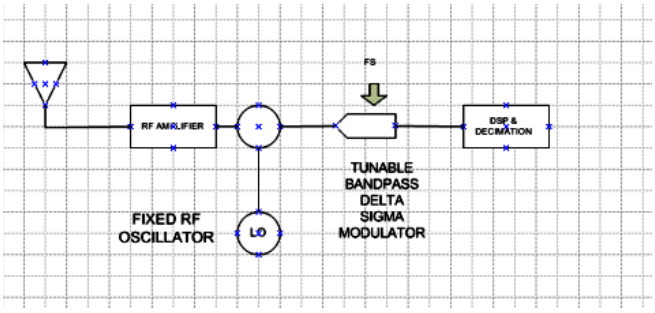

Fig 3.3 (a)A Tunable Bandpass modulator with introduction of channel selection in intermediate frequency.

The modulator created by this method consists of an active inductor circuit,an OTA,a comparator and a current steering DAC.In fig 3.3 (b) Transistors M4 have negative Gm while M5-M9 have positive Gm.Mp is behaving as a resistor.The cascade topology used in this active inductor topology [5]increases the output impedance which in further is reducing the series resistance of RLC series network. Inductance expression can be written as

$$L = \frac{C1(1 + gm1Rex)}{gm1gm2}$$

Rex is Mp resistor and

Thus the inductance is increased by a factor (1+gm1Rex) which in turn increases the quality factor with a minuscule increase in noise.

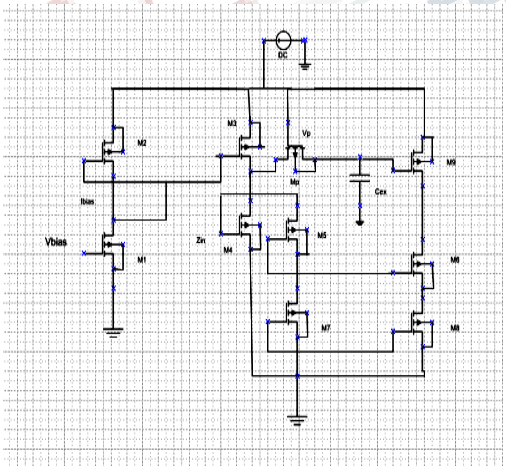

Fig 3.3(b) Active Inductor Topology

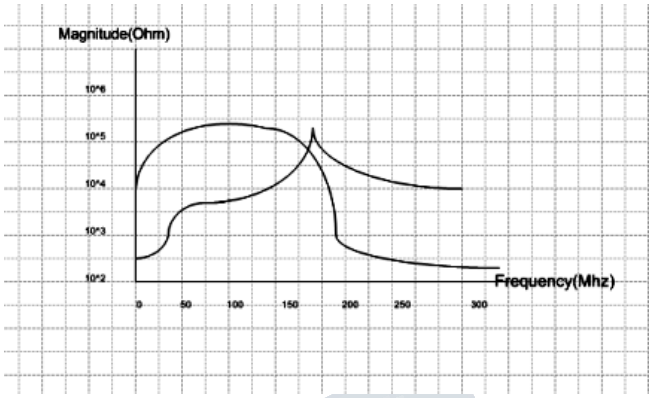

Fig 3.3 (c) Active Inductor Frequency Response

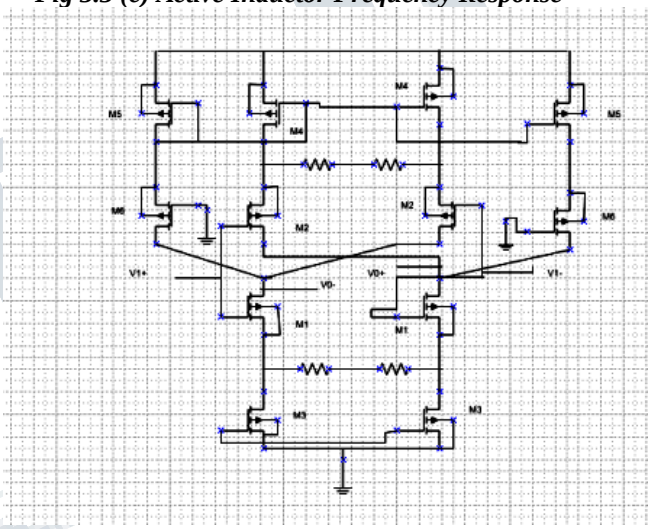

Fig 3.3(d) OTA

OTA structure increases transconductance and power efficiency**.**

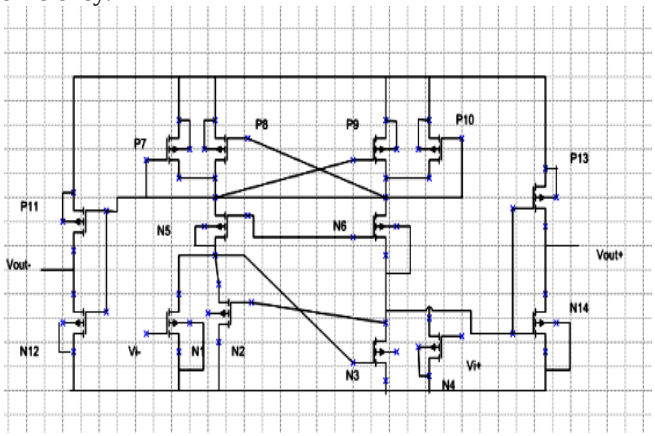

Fig 3.3(e) Comparator

Quantizer has been formed with a dynamic D flipflop and sample and hold comparator function. A DAC has been used for taking output from the comparator

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 8, August 2017

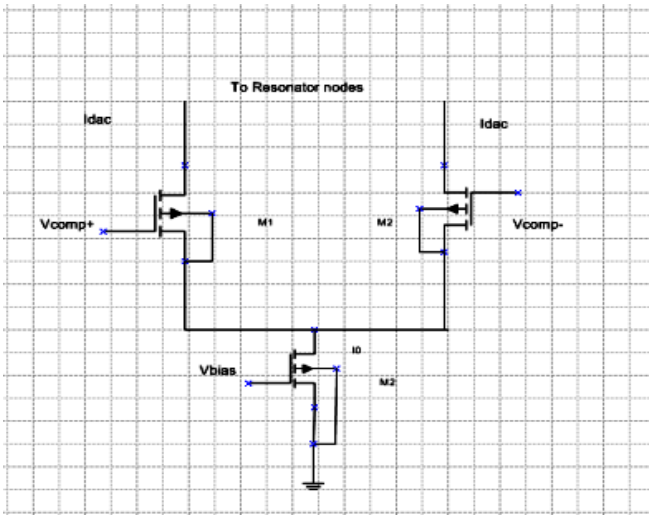

Fig 3.3(f) Current Steering DAC.

A diiferential circuit is used with NRZ feedback

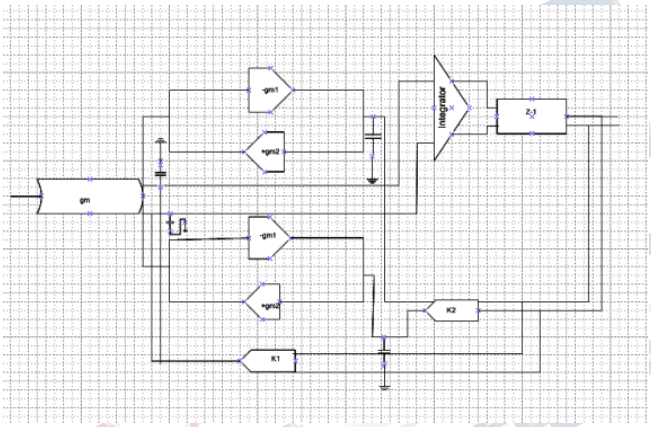

FIG 3.3(g) CTDSM

In this complete methodology the centre frequency of the modulator has been enhanced and SNDR has also been increased.

Excess loop delay compensation is done by addition of a latching stage after the quantizer,but at high frequencies DAC is contributing more to the loop delay.Hence modification in transfer function includes eliminating at frequency when loop delay is equal to sampling frequency.

(IV)

A hybrid delta-sigma modulator [6] is used for higher order loop filtering with digital circuits.With the help of an additional noise coupling block [Table I] ELD is compensated.

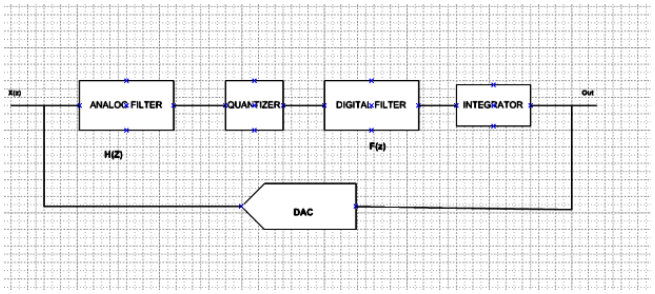

Fig3.4 (a) Hybrid Delta Sigma Modulator

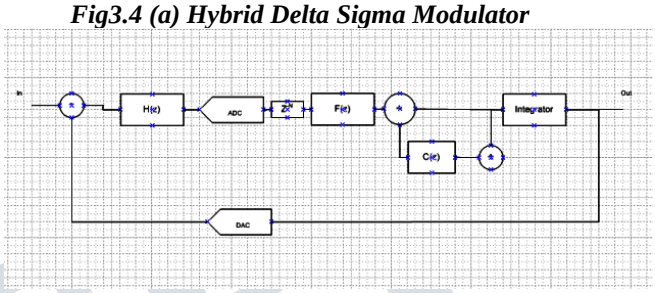

Fig 3.4(b) Noise Coupling Block Model

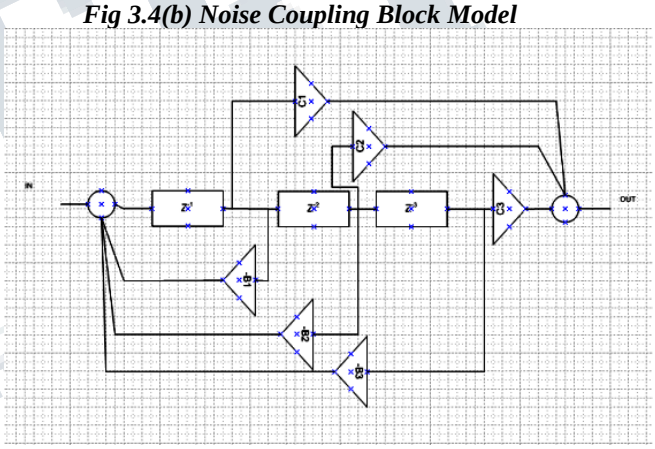

Fig3.4(c) Noise Coupling Block

(V)

Here[7] the operation is performed in two stages. Stage I quantizer error is extracted by Stage II and processed and an qauntizer with a error is added to Stage I.The error in processing and extraction of Stage I qunatizer error is called as ESLD. The proposed SMASH TI crossed coupled modulator[7] is used for ELD compensation.e1 and e2 cancel each other.But,processing of e1 and e2 through stage 2 quantizer and loop filter to generate an output y11 and y22 is impossible.So,a unit delay is introduced between stage I quantizer including both paths and coupling point of stage II output. For compensation of delay a fast path is added around stage I around quantizer ,and an additional cross coupled path is introduced by a polynomial,C(z).

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 8, August 2017

$$C(z^{-1}) = -z^{-3} + 5z^{-2} - 7z^{-1} + 3$$

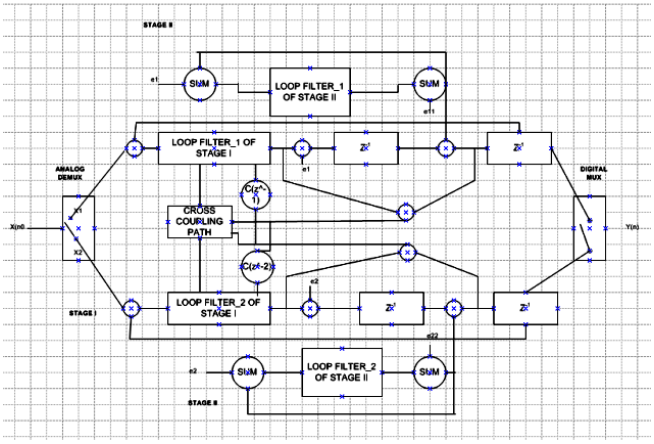

Fig3.5 Sturdy multistage noise shaping architecture

IV. TRANSFER FUNCTION MODIFICATION

Sn	ORIGINAL TRANSFER FUNCTION	MODIFIED TRANSFER FUNCTION
I (A)	$H(s)=\frac{K1(S)+K2(S)}{S^2}$	$H(s)\times e^{St}$
I (B)	$\frac{H(s)}{} = \frac{K1}{S} + \frac{K2}{S} + \cdots \ldots \frac{kn}{s}$	$H(s)=\frac{K1}{s}\times e^{St} + \frac{K2}{S}e^{St} + \cdots \frac{kn}{s} \times e^{St}$
III	$H(s)=\frac{gmC(1+gmRex)s+gm}{s^2+\frac{gm1gm2}{c^2(1+gm1Rex)}}$ $\frac{H(s)}{} = \frac{H2z^2+H1z+H0}{z(z^2-2zcosO+1)}$	$H2 = \frac{1}{\theta(K2cos(\theta-\theta td)-k2-k1sin(\theta-\theta td)}$
IV	NTF(c)	$\frac{NTF(z)}{} = \frac{1-C(z)}{1+z^{-N}-NH(z)F(z)}$

TABLE I TRANSFER FUNCTIONS OF THE ANALYZED CIRCUIT

V. CONCLUSION

We had provided a jist of different compensation techniques used for excess loop delay in a continuous time delta sigma modulator.The circuit analysis has been done in order to restore the Noise Transfer function by tuning of the filter coefficient.As the Excess loop Delay is compensated it causes an increase in SNR which causes a further increase in resolution.Hence by maintaining these tradeoffs the performance of continuous time Delta- Sigma Modulator can be improved.

VI. APPENDIX

In this appendix we will derive the dependency of SNR on excess loop delay .Referring to Fig 1.2,the error singal can be written as e(n)= $\frac{td}{Ts}\,y(n)-y(n-1)$.The power of e(n) in the signal band is $J(m)=\frac{4p}{OSR}(\frac{td}{Ts})^2$.Here p=0.8(ideal) probability that latch makes the transition.Let us assume the input signal x(n)=Acos$(2\pi fint)$,thus the inband SNR due to metastability as SNR=10log$\frac{A^2.OSR.T^2}{8.p.td^2}$.Thus the signal dependent delay of the comparator causes a low frequency noise floor which is degrading the SNR.Thus as we compensate the Excess Loop Delay ,SNR is improved and hence the performance of the of continuous time Delta Sigma modulator.

REFRENCES

[1] Delta Sigma Data convertors by Steven R Norsworthy,RichardSchreier,Gabor C Temes, IEEE Press.

[2] High-Speed Data Conversion Using Continuous-Time Delta-Sigma Modulators by James A. Cherry.

[3] Excess Loop Delay Compensation in Continuous-Time Delta-Sigma Modulators -Shanthi Pavan.

[4] A Continuous-Time ΔΣADC Utilizing Time Information for Two Cycles of Excess Loop Delay Compensation-Yue Hu, HariprasathVenkatram, Nima Maghari, and Un-Ku Moon

[5] A 400 MHz Delta-Sigma Modulator for BandpassIF Digitization Around 100 MHz With Excess Loop Delay Compensation -AkhilGupta, Shahrokh Ahmadi, Mona Zaghloul Department of Electrical and Computer Engineering The George Washington University Washington, DC, USA

[6] Extra Loop Delay Compensation for Hybrid Delta-Sigma Modulators Yusaku Hirai, Kenji Ohara, and Toshimasa Matsuoka Graduate School of Engineering Osaka University, Osaka, Japan

[7] A Novel Excess Sturdy-MASH-Loop-Delay Compensated Cross-Coupled Modulator, 2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded SystemsJ. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.

[8] David A.Johns, Ken Martin, "Analog Integrated Circuit Design" John Wiley & Sons In.

[9] Behzad Razavi, "Principles of Data Conversion System Design" Wiley-IEEE Press

[10] R.Jacob Baker "CMOS circuit design layout and stimulation",IEEE Press

[11]Understanding Delta Sigma Convertors,by Shanti Pawan,Richard Schreier,Gabor C.Temes. [12] US Patent Pipelined delta sigma modulator analog to digital converter ,US 20050083220 A