

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE) Vol 4, Issue 7, July 2017 Design of Nikhilam Sutra And Reversible Logic For Vedic Multiplier

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Abstract: — In this paperNikhilam Sutra of Vedic mathematics and Reversible Logic is discussed which are helpful in improving the performance of Multipliers.

Keywords-Vedic Mathematics, Nikhilam Sutra and Reversible Logic..

I. INTRODUCTION

Multiplication is an important function in arithmetic operations. Multiplication time is the dominant factor in determining the instruction cycle time of a DSP chip. Demand for high speed processing is increasing as a result of expanding computer and signal processing applications. Where as in handheld and compact electronics devices power consumption has became very critical factor. Therefore, reducing the time delay and power consumption is of great importance in DSP as well as in general processors. Vedic methods have shown great importance in reducing the time delay of the multipliers[1], where in the reversible logic is helpful in reducing the power consumption of the digital circuits.

II. VEDIC MATHEMATICSAND REVERSIBLE LOGIC

A. Vedic Mathematics

Veda is a Sanskrit word derived from Vid, meaning to know without limit. Word Veda covers all Vedasakhas (branches) known to humanity. Founded by Swami Bharati Krishna Tirtha (1884-1960), proposed by former Jagadguru Sankaracharya of Puri culled a set of 16 Sutras (formulae's) and 13 Sub - Sutras from the Atharva Veda, which deal with various fields of mathematics such as algebra, geometry, calculus etc. In Sanskrit, the word Sutra stands for "Thread of Knowledge". He developed methods and techniques for amplifying the principles comprised in the sutras and their sub-sutras, and called it Vedic Mathematics. The calculation methods are based on pattern recognition and hence allows for constant expression of a student's creativity, and it is to learn. The choices made and the choices have to be made at each stage of the calculation keeps the minds lively and alert, hence a universal development of the human brain

automatically takes place. Though the solutions appear like magic or in fraction of time, the application of the Sutras is perfectly logical.

Nikhilam Sutra is a method used for multiplication. Nikhilam sutra is known as "All from 9 and the last from 10". The sutra can be very effectively applied in multiplication of numbers, which are nearer to bases like 10, 100, 1000 and so oni.e., to the power of 10. The procedure of multiplication using the Nikhilam involves minimum number of steps, space, time saving and need only intellectual calculation. The numbers to be multiplied can be either less or more than that of the base considered. The difference between the number and the base is known as deviation, this deviation may be either positive or negative. The positive deviation is defined without the positive sign and the negative deviation, is defined using rekhank (a bar on the number).

Steps involved in solving problems:

4.

1. Find the nearest base of both the numbers in power of 10.

2. Subtract both the numbers from respective bases.

3. Find the multiplication value between the two subtracted numbers.

Find the common the difference.

5. Combine step 2 and step 4 answers to get the final output.



Figure 1: Nikhilam Sutra Example 1

Figure 1 shows the details of the parameters of Nikhilam Sutra calculation.



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Step 1: Select the nearest base as 100 for both 98 and 97.

Step 2: Subtract both the numbers from the base i.e., 100-98=2 and 100-97=3.

Step 3: Finding multiplication between two subtracted values i.e., 2x3=6.Here, the result is 1 digit which did not satisfy the Nikhilam rule. The rule says, the result must have the digits equal to the zeros in the selected base, in this case it two (i.e., two zeros in 100). Hence, write down 06 on the RHS side.

Step 4: Finding common difference i.e. 98-3 or 97-2 the difference will be same for both scenarios i.e. 95. Write down this on the LHS of the previously written value.

Step 5: Writing these two values together will give the final answer as 9506.

ii. Multiplying 88 by 66.

When the vertical multiplication of the deficit digits (for obtaining the RHS portion of the answer) gives a product consisting of more than two digits when base is 100, then the surplus portion of the left must be carried over to the left of the dividing line. For multiplying 88 times 66 then the number 408 in the RHS portion of the product contains place values as units, tens and hundreds, where as needed is only units and tens i.e. 08. Therefore, the digit having place value as hundred i.e. 4 will be added to the LHS result on the left of the dividing line. The result will become $54+4 \mid 08$ i.e., 5808.



Figure 2 shows the details of the parameters of Nikhilam Sutra calulation.

Hence Vedic mathematics is fun and fluent to learn, faster to use and less liable to fallacious than conventional methods. This sutra can be used for the multiplication of binary numbers and the multiplication formula can be applicable to all types of multiplications. In Vedic multiplier the computation time is less when compared with other multipliers [2]. Due to its regular structure it can be realized easily in a silicon chip.

The Multiplier design and mathematical expression using Nikhilam sutra to solve the binary numbers is as shown in figure 3.



P=X*Y=2^k2(X+Z2*2^(k1-k2))+Z1*Z2. Figure 3: Mathematical Expression and Multiplier Architecture for Nukhilam Sutra. BSM - Base Selection Module PID - Power Index Determinant

B. Reversible Logic

Design logic that does not result in information loss is called reversible logic. Reversible logic naturally takes care of heat generated due to information loss. Bennett showed [3] zero energy dissipation would be possible only if the network is built with reversible logic gates. Energy loss is an important consideration in digital circuit designs. A part of this problem arises from the technological non-idealistic switches and materials. The other part of the problem arises from Landauer's principle for which there is no solution. Landauer's Principle [4] states that the logical computational circuits that are not reversible necessarily generate k*T*ln*2 joules of heat energy, where k is the Boltzmann's Constant k=1.38x10-23 J/K, T is the absolute temperature at which the computation is performed. Although this amount of heat appears to be small, Moore's Law predicts exponential growth of heat generated due to continuous information loss, which will be a noticeable amount of heat loss in next decade. Thus reversibility will become an essential property in future design technologies.

Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine.



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Reversible logic is one of the promising fields for future low power design technologies. Reversible logic gate is used to design energy and power efficient ALU.

Reversible gate can generate unique output vector from each input vector and vice versa, i.e., there is a one to one mapping between the input and output vectors. Thus the number of outputs in a reversible gate or circuit has the same as the number of inputs. Commonly used traditional NOT gate is the only reversible gate. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.



igure 4: General Structure of Reversib Circuit/Gate.

General structure of reversible circuit/gate is shown in figure 4. Garbage outputs are those which do not contribute to the reversible logic realization of the design engine. Quantum cost is the cost of the circuit in terms of the cost of a primitive gate. Gate count refers to the number of reversible gates used to realize the function. Gate level is the number of levels which are required to realize the given logic functions. Example:Feynman Gate.



Figure 5: Quantum representation of Feynman Gate.

Figure 5 shows the quantum representation of the Feynman gate. It is a 2x2 gate i.e. 2 input and 2 output gate and its logical circuit mapping is (A, B) to (P=A, Q=A \oplus B). From table 1 [5] Feynman gate output can be described as when A=0 then Q=B, when A=1 then O=~B.

Table	i.	Feynman	gate	truth	table.

Α	B	Р	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Here A is the controlling input and B is the controlled input, P and Q are the two outputs. It is known as Controlled NOT (CNOT) Gate. The quantum cost is 1 and is generally used for Fan Out purposes.

Such reversible logic gates are very effective in minimizing power consumption of the logical circuits [6].

III. CONCLUSION

The survey has explained how the adoption of Vedic mathematics into logical circuits is helpful in increasing speed of the multipliers and the adoption of reversible logic is helpful in designing the energy efficient logical circuits.

REFERENCES

[1] Vedic Mathematics or Sixteen Simple Mathematical Formulae from the Vedas By Jagadguru Swami Sri Bharati Krsna Tirthaji Maharaja, Sankaracharya Of Oovardhana Matha, Puri.

[2] Pawan Kumar, Sai Prasad Goud, "FPGA Implementation of high speed 8-bit Vedic multiplier using barrel shifter", 978-1-4673-6150-7/ ©2013 IEEE.

[3] C.H. Bennett, "Logical Reversibility of Computation", IBM J.Research and Development, pp. 525-532, November 1973.

[4] R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp. 183-191, 1961.

[5] "Design Methodologies for Reversible Logic Based Barrel Shifters", Saurabh Kotiyal, University of South Florida, January 2012.

[6] Rakshith Saligram and Rakshith T.R "Optimized Reversible Vedic Multipliers for High Speed Low Power Operations" Proceedings of 2013 IEEE Conference on Information and Communication Technologies (ICT 2013).