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Design and Implementation of cascaded H-Bridge Multilevel inverter using digital control schemes

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***Abstract* - the objective of the present work is to obtain a three level ac output, which is obtained by a 4-stage, 3-level multilevel inverter. An inverter receives dc supply for its input and produces ac output. It stepped up to 220 V, 50 Hz single-phase ac supply with the help of a step up transformer with E/I core with a resulting given input of 12V. Using a simple L-C filter at the rectifier output terminals the obtained dc supply can be made ripple free. The circuit consists of 4 MOSFET's which requires more current and generate heat and to dissipate heat sink, which is fabricated in aluminum. The obtained dc from the renewable sources i.e., Solar Panel, Wind Mill and Hydro Mill is directly fed to the dc to dc converter which boost up the input power and this is fed to the battery with the capacity of 12V, 24 AHC. Simulation of the firing pulse generation circuit and multilevel inverter was done using MATLAB 13a and Simulink. Since we are using Hybrid inverter, to establish the communication, ARM Processor (LPC2148) and GSM (SIM900A) module is used to provide access of the user to the model i.e., controlling its mode of control of operation.**

***Keywords:* Multi-Level Inverter, Matlab13a Simulink, PWM, Diode Clamping..**

INTRODUCTION

The multilevel inverters have drawn tremendous interest in the power industry. They present a new set of features that are well suited for use in reactive power compensation. It may be easier to produce a high power high voltage inverter with the multilevel structure because of the way in which device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverter without requiring higher rating on individual devices can increase the power rating of the overall circuit. As the no of voltage levels increases the harmonic content of the output voltage waveform decreases significantly here the dc input to the multilevel inverter is obtained by renewable sources of 12V input to 220 V, 50 Hz single-phase ac supply. Using a simple R-C filter at the rectifier output terminals the obtained dc supply can be made ripple free. The circuit consists of 4 MOSFET's which requires more current and generate heat and to dissipate heat sink, which is fabricated in aluminium.

To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require various pulse width modulation (PWM) strategies, which increase the switching frequency of the power devices. In the case of multilevel inverters, as the number of voltage levels increases the harmonic content of the output voltage waveform decreases, even without using any pulse width modulation technique. As the switching frequency is reduced the power losses are also minimized, and thereby increasing the efficiency of the system.

Since the early years high power line commutated thyristor in conjunction with capacitors and reactors have been employed in various circuit configurations to produce variable reactive output. Using appropriate switch control the VAR output can be controlled continuously from maximum capacity to maximum inductive output at a given bus voltage.

SIMULATION ANALYSIS

The switching states of the lookup table shown in table 1 can be obtained from the repeating sequence stair available in the sources block. Here the DC voltage of 12V has been into 12V battery sources. The output voltages are taken across the resister of 1000 ohms. For the switches S1, S2, S3 and S4 different modes of operation of three level cascaded H-Bridge multilevel inverter are explained below:

Mode 1:- In this mode of operation of three level cascaded H-Bridge inverter switches s1 & s2 are turned on & no source is connected to the load .Zero output voltage across the load is obtained.

Mode 2:-In this mode of operation of three level cascaded H-Bridge inverter switches s1 & s4 are

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turned on. Output voltage obtained across the load is +V dc.

Mode 3:- In this mode of operation of three level cascaded H-Bridge inverter switches s2 & s3 are turned on. Output voltage obtained across the load is –V dc.

Mode 4:- In this mode of operation of three level cascaded H-Bridge inverter switches s3 & s4 are turned on. Output voltage obtained across the load is zero. The

Same operation is shown in tabular form below in table 1.Table 1 Modes of operation of single phase three level cascaded H-Bridge Inverter

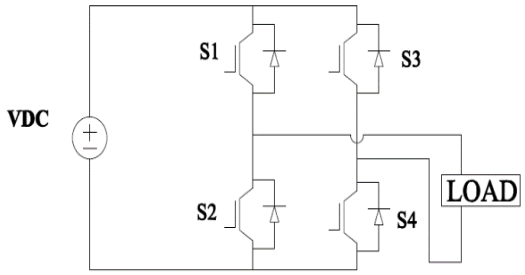

Fig 1: Block Diagram of 3 level multilevel Inverter using power semiconductors.

MODE	S1	S2	S3	S4
1	1	1	0	0
2	1	0	0	1
3	0	1	1	0
4	0	0	1	1

Table 1: Switching Sequence.

These switching pulses are drawn from a PWM Generating circuit which is according to the behaviour of the main circuit. The characteristics required are:
1. Frequency of voltage applied at the inverter terminals should be same as the frequency of the source voltage. For this to happen, PWM is generated taking reference from source voltage.
2. The switching pulses should be given such that the resultant waveform should have average values for each pulse resulting in a sinusoidal waveform.
3. One pair of switches has to give switching pulses while the other pair has to be in idle state or off state.

For PWM to have the first characteristic a sample has to be taken from the source itself for frequency. For the second characteristic to be satisfied we need to use a signal generator and the best source of sine wave that can be thought of is the source waveform itself. So the source voltage waveform is selected as reference.
The source voltage waveform is obtained by using a voltmeter at the source. A transport delay block is used for getting a delay between source voltage and Inverter voltage. The output of the delay block is given to PWM sub circuit
In PWM sub circuit we used a block provided by MATLAB. This block will give the pulses with duty cycle proportional to the instantaneous value of the reference.

Duty Cycle = $\frac{V+1}{2}$

Where V is the instantaneous value

(i.e.) when V is negative, duty cycle <50% when V is positive, duty cycle>50%

When V is zero, duty cycle = 50%

But the voltage waveform of source starts from the instantaneous value zero. For instantaneous value ‘0’ the duty cycle will be 50% which is undesirable. So a waveform has to be generated such that, for voltage waveform starting at 0 another waveform has to start at 1 corresponding to the original waveform. PWM input has to reach peak with the source waveform and has to reach -1 when source waveform reaches 0. This is followed by the source expression “-cos2θ”. So we squared the source waveform by using the multiplication block. Then remove the DC offset half by subtracting the above result with half. Then we multiplied it with a gain two because the waveform is now which is having half the amplitude required. So when a gain of two is applied it becomes - cos2θ. Now this can be used as reference to the PWM block provided by the MATLAB.
Now we need to separate the switching pulses for the pair of switches S1, S4 and the other pair S2, S3 so as to follow the 3rd characteristic. For this, we developed a circuit where one output is a square waveform. This reaches +1 during the positive half cycle of source waveform and reaches 0 during the negative half cycle of the waveform. The other output is vice versa of the above i.e., it will reach 0 for the positive half cycle of

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the source waveform and reaches +1 for the negative cycle of the waveform.

The first output is multiplied with the PWM pulses and is given to the pair S1, S4 switches. The second output is multiplied with the PWM pulses and is given to the pair S2, S3 switches. This is how PWM is being generated.

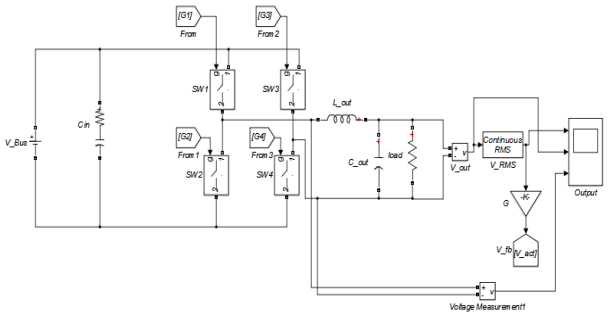


Fig 2: Simulink model for three leg operation of a 3 level Multilevel inverter

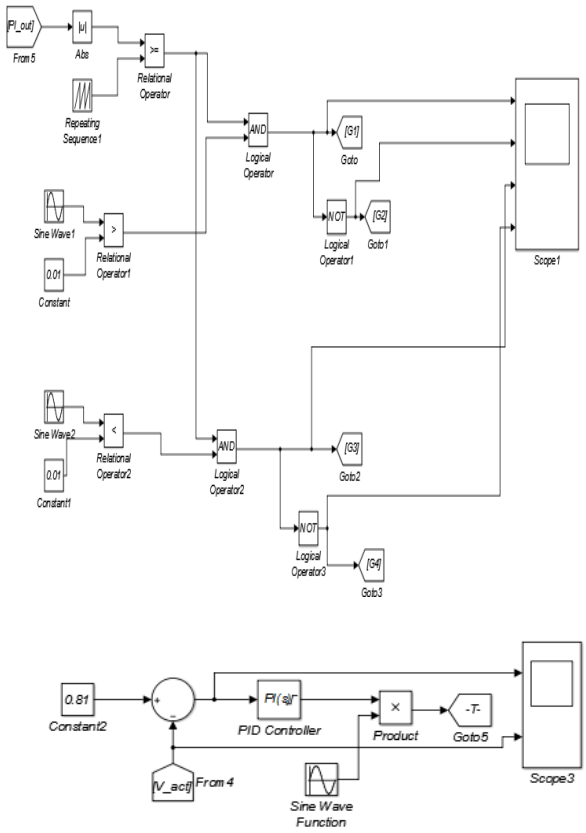
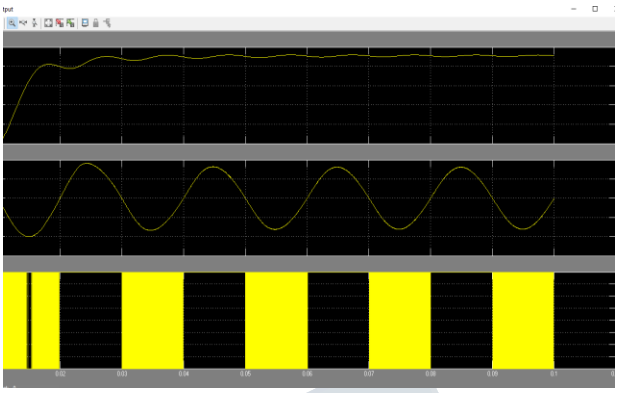


Fig 3: Simulink model of a 3 level multilevel inverter with Digital control scheme.



III. RESULTS

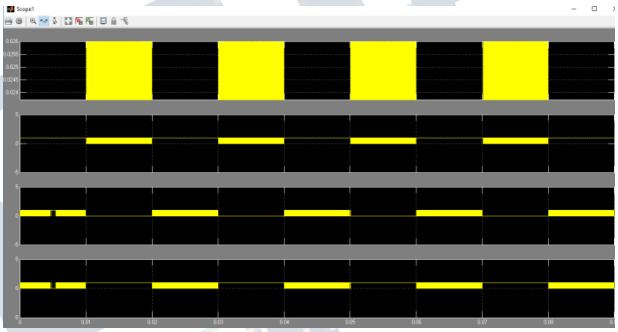


Fig 6: Simulink model for Reactive Power Compensation Using PWM Technique.

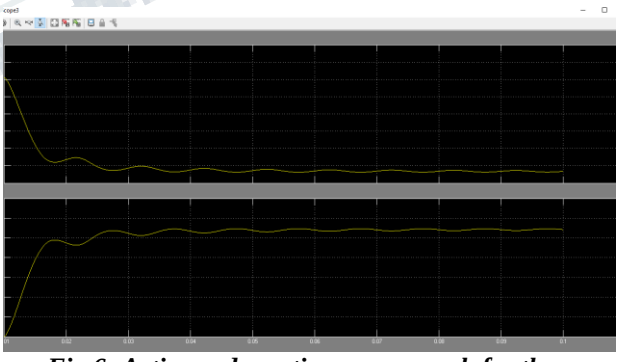


Fig 6: Active and reactive power graph for the reactive power compensation for 3 level multilevel inverter.

IV. CONCLUSIONS

The utilization of multilevel inverters has increased in the last decade eliminating the necessity of AC output filter devices such as inductors, capacitors etc. We will be designing a hybrid power system as everyone uses power from grid. Customers will be able to offset their power usage over an entire billing period as the power transmitted to them will be sourced from a supply of 800-1K watts of power generated using renewable sources of energy. The residual power available with us after our consumption will be supplied to the grid (government) in exchange for money. This project will be simulated using design analysis. Waveforms simulation would be done with the help of MATLAB. This topology reduces the output harmonics as well as the cost. The proposed multilevel inverter provides higher output quality with relatively minimal power loss as compared to the other conventional inverters.

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AUTHOR PHOTOS AND BIOGRAPHY

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