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Design of Capacitor-less Low Drop-out Voltage Regulator for 100mA Load Current in 90nm Technology

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Abstract: **A capacitor-free CMOS low-dropout regulator (LDO) for system-on-chip applications to reduce board space and external pins is presented. The 1.5 V LDO with a power supply of 1.8 V with settling time of 0.5 µs is implemented in GPDK 90nm CMOS technology for load currents up to 0 -100 mA with a drop-out voltage of 300 mV. Simulation results show that the LDO achieves a PSR of -43.741 dB up to 1 kHz and -39.130 dB up to 1MHz. The LDO achieves Line regulation of 6.38mV/V and Load Regulation of 0.027 mV/mA. The proposed LDO design has less output ripple, fast transient response, and achieves current efficiency of 83.33%. T he area acquired by the layout of the design is approximately equal to 0.0299µm2 .Thus, the presented capacitor-less LDO voltage regulator is suitable for SoC solutions.**

Index Terms— Capacitor-less, low drop-out regulator (LDO), power supply rejection (PSR), System on Chip (SoC).

I. INTRODUCTION

A tremendous increase in the usage of battery operated portable devices led the designers to focus on the power management skills and SoC solutions [1]. The study of power management techniques has increased spectacularly within the last few years. Integration of power management into a single system-on-chip improves device power efficiency resulting in extended battery life and operation life. A power management circuitry consists of linear regulators (mainly LDOs), switching regulators such as buck, boost converters and charge pumps and digital control logic. Due to high accuracy and efficiency of Low Dropout Regulators (LDOs) under the class of linear regulators, LDOs are widely used in portable applications like mobile phones, PDAs [2]. The principle requirements of these applications are small size, high integration and low cost [3]. These portable applications demand high power efficiency and low output voltage ripple.

Due to the emerging need of high-performance low voltage LDOs for low-voltage mixed-signal systems, many researchers have recently proposed many advanced methods to improve the performance of LDOs. LDOs supply current to analog/base band, digital, and RF circuits like LNA, VCOs and PA [4] which demand a clean and fixed voltage even if there are fluctuations in input voltage. Rincon-Mora *et al.* proposed current-efficient voltage buffer, forward-biased power transistor, pole-zero doublets for load-regulation enhancement, and capacitance multiplication [5].

LDOs, especially for the low-voltage LDO designs. Moreover, the off-chip capacitor, which is the key for stability and high LDO performance, cannot be eliminated. This off-chip capacitor is the main obstacle to fully integrating LDOs in system-on-chip designs.

As a result, low-voltage high-stability and fast transient LDOs with, preferably, capacitor-free operation should be developed. Solving the correlated tradeoffs on stability, precision, and recovery speed is the main challenge of capacitor-free LDO design [6].

In this paper, a CMOS LDO that is targeted for CMOS system-on-chip designs is presented. The circuit architecture is based on a three-stage amplifier design [7], and it provides a capacitor-free feature to eliminate the need of bulky off-chip capacitor. Both fast load transient response and high power-supply rejection ratio (PSRR) are achieved due to the fast and stable loop gain provided by the proposed LDO Structure. The power pMOS transistor in the proposed LDO operates in linear region at dropout, and hence, the required transistor size can be reduced significantly for the ease of integration and cost reduction. In addition, a novel CMOS voltage reference based on weighted difference of gate – source voltages enables full-CMOS implementation.

This paper focuses on low-dropout (LDO) voltage regulators. LDO regulators are an essential part of the power management system that provides constant voltage supply rails. They fall into a class of linear voltage regulators with

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improved power efficiency. Efficiency is improved over conventional linear regulators by replacing the common-drain pass element with a common-source pass element to reduce the minimum required voltage drop across the control device. Smaller voltage headroom in the pass element results in less power dissipation, making LDO regulators more suitable for low-voltage, on chip, power management solutions.

II. CAPACITOR - LESS LDO

A low drop-out voltage regulator ideally produces a constant output voltage regardless of supply voltage or load current variations. Fig. 1 shows a simple two pole capacitor-less LDO architecture consisting of error amplifier, pass transistor and a feedback network. The input voltage is applied to the pass transistor which generally operates in linear region to drop the input voltage Vin down to the desired output voltage. The resulting output voltage is sensed by the error amplifier and compared to a reference voltage. The error amplifier drives the gate of pass transistor to the appropriate operating point to get desired output. To compensate the absence of a large external capacitor, a capacitor-less LDO requires an internal fast transient path. Power efficiency of LDO is directly proportional to the drop-out voltage (VDO) which is the difference between input and output voltage. It is given as;

$$\eta = \frac{V_{out} * I_{out}}{V_{in} * I_{in}} = \frac{(V_{in} - V_{do}) * I_{out}}{V_{in} * (I_q + I_{out})} \qquad (1)$$

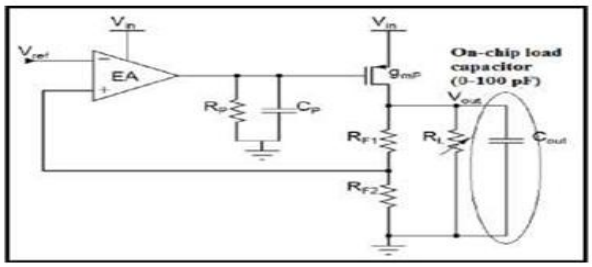

Fig 1: External capacitor-less LDO voltage regulator.

Where, IQ is the total quiescent current of the circuit, Vin is the input power supply, Iout is the load current and Vout is the regulated output.

From Eq. (2) Vout depends on the reference voltage Vref.

$$V_{out} = \left(\frac{A_{OL}}{1 + A_{OL}}\right)\left(1 + \frac{R_{F1}}{R_{F2}}\right)\left[V_{ref} + \frac{V_{in}}{A_{EA}}\right] \qquad (2)$$

Here, AOL is the open loop gain of LDO and AEA is the gain of error amplifier. By assuming AOL >>1, Eq. 2 can be rewritten as:

$$V_{out} = \frac{V_{ref}}{\beta} + \frac{V_{in}}{A_{\alpha} * \beta}, \qquad \beta = \frac{R_{F2}}{R_{F1}+R_{F2}} \qquad (3)$$

Where, β is the feedback ratio.

For open loop stability of the LDO, the loop is usually broken in the feedback. For better line and load regulation AOL is required. The effective output resistance Rout of LDO is the parallel combination of resistance of pass transistor MP, total feedback resistance (RF1 + RF2), and the load resistance RL. It is evident that for a given channel length modulation factor (λ), load current is inversely proportional to output resistance Rout. The pass transistor used in LDO is generally of a huge size as it is designed for low drop-out which means lower VDSAT at maximum current. Due to huge W/L ratio of pass transistor it constitutes parasitic capacitance (CP = CgsP + gmPRout * CgdP) at its gate which in turn affects slew rate time (tSR) of LDO as shown in Eq. (4).

$$t_{SR} = \frac{C_p \Delta V_p}{I_{SR}} \qquad (4)$$

Where ΔVP is the voltage variations across CP and CgsP and CgdP are gate-source and gate-drain parasitic capacitance of pass transistor.

The specifications of the LDO can be classified into three classes: 1) static-state specification; 2) dynamic state specification; and 3) high-frequency specification. Line and load regulations, as well as temperature coefficient, are regarded as static-state specifications, while line and load transient responses, as well as ripple rejection ratio, are dynamic-state specifications. The high-frequency specifications are PSRR and output noise. All specifications are correlated, and they have tradeoffs with the LDO stability when dominant-pole compensation with pole-zero cancellation is used. Line and load regulations are two important specifications that relate to the output-voltage accuracy. PSRR depends highly on both loop-gain bandwidth and ESR. An LDO with a good PSRR and line transient response results in a good ripple rejection ratio. Therefore, an advanced LDO structure which solves the

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tradeoff problems of classical LDOs, is presented in next section.

III. PROPOSED LDO STRUCTURE

The proposed LDO consists of an error amplifier, second stage amplifier and pass transistor in the forward path and resistive feedback (β) network in the feedback path as shown in Fig. 2. However, classical two-stage-amplifier topology is not optimum since the power transistor cannot function as a high-gain stage in dropout condition. Instead, an LDO can be viewed as a three-stage amplifier with the power transistor as the last stage.

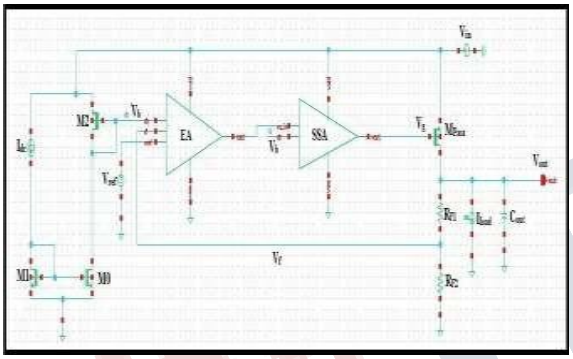

Fig 2: Proposed capacitor-less LDO's architecture.

A. Error Amplifier (EA)

The first stage of capacitor-less low dropout voltage regulator is the Error Amplifier stage. Fig.3 shows the Error Amplifier circuit setup. The Error Amplifier is a common differential amplifier which amplifies the difference in the two inputs. The presented Error Amplifier is a PMOS input differential pair which requires 5µA of current and the offset is 5mV. Here the negative terminal is given from the reference

voltage which is from the voltage source (0.3V) and the positive terminal is given from the feedback network. The output of the Error Amplifier stage is the input for the second stage. Assuming appropriate overdrive voltages for each branch and using Eq. (5), one can calculate the aspect ratios of each transistor.

$$ID = (1/2)\ \mu n,pCox\ (W/L)i(Vov)2 \qquad (5)$$

Where i = 1, 2, 3...

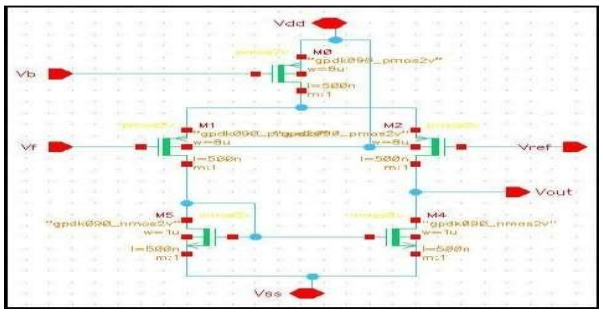

Figure 3: Error Amplifier Circuit Setup

B. Second Stage Amplifier (SSA)

The second stage of capacitor-less low dropout voltage regulator is the Second stage Amplifier. Figure 4 shows the Second stage amplifier circuit setup, which is the done by cascading the gm boosting stage and the second stage. The second stage provides a high gain which will be useful for capacitor multiplication for the pole-zero compensation. This stage requires 30µA of the total current. This stage is the biasing input to the pass transistor stage. It will helpful to fix the operating point for the pass transistor stage.

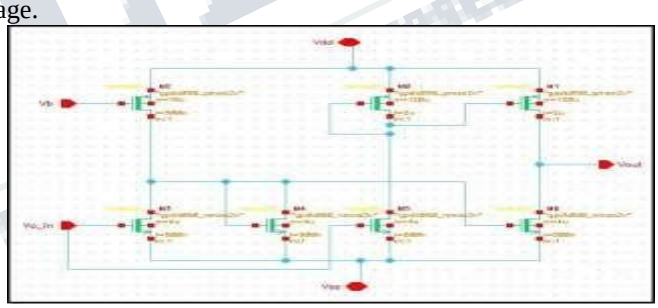

Figure 4: Second stage amplifier Circuit Setup

C. Pass transistor

The major design issue to be considered in the design of capacitor-less low dropout voltage regulator is the PASS TRANSISTOR stage. Figure.5 shows the circuit set up of pass transistor stage. The pass transistor size should be large in order to drive the large load current. To find the size of the pass transistor, the gate should be biased with a proper voltage in which the pass transistor should be in saturation region and the required VDSAT should be measured for the maximum load current. The Quiescent current should also be considered which should be less for this stage. It can be reduced by increasing the resistor values.

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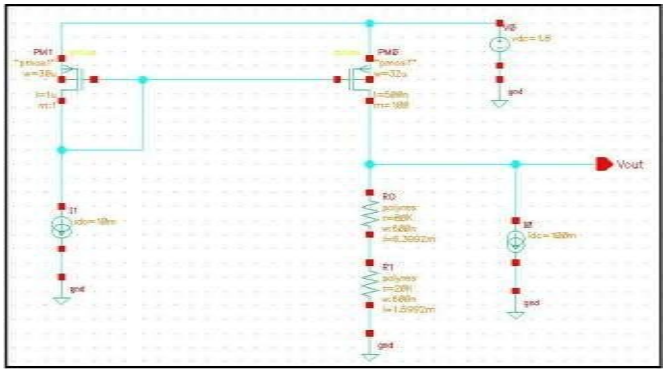

Figure 5: Pass Transistor Circuit Setup

The drop-out voltage of 300 mV is chosen in this paper for a maximum load current of 100 mA as shown in Fig. 5. The size of the pass transistor is decided from the drop-out voltage using relation;

$$V_{dropout} = V_{DSAT} = \sqrt{\frac{2I_{MAX}}{\mu_p C_{ox}(W/L)}} \quad (6)$$

Rewriting Eq. (6),

$$\frac{W}{L} = \frac{2I_{MAX}}{\mu_p C_{ox} V^2_{DSAT}} \quad (7)$$

Fig. 6 shows the transistor level design of the proposed LDO architecture being implemented in GPDK 0.90µm technology. Feedback resistors RF1 and RF2 are designed such that they follow the Eq. (8).

$$V_{OUT} = V_{REF}\left(1 + \frac{R_{F1}}{R_{F2}}\right) \quad (8)$$

Also,

$$R_{F1} + R_{F2} = \frac{V_{OUT}}{I_a} = \frac{1.5V}{15\mu A} = 100K\Omega \quad (9)$$

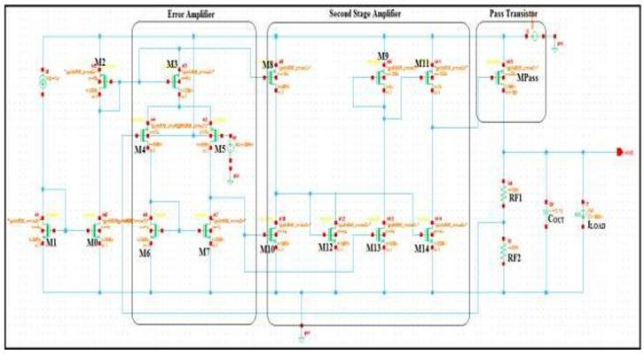

Fig 6: Schematic of proposed LDO architecture.

And,

$$R_{F2} = \frac{V_{ref}}{V_{out}}(R_{F1} + R_{F2}) = \frac{0.3V}{1.5V} * 100K\Omega = 20K\Omega \quad (10)$$

From equations (9) and (10), R_{F1} will be 80K Ω

Table i. Transistors aspect ratios

Transistor'	*W*	*L*	*Bia*
M0, M1	4	500n	5
M2,M3	8	500n	5
M4,M5	8	500n	2.
M6,M7	1	500n	2.
M	16	500n	1
M9,M11	120µ	2	1
M10,M12	4	500n	1
M13,M14	4	500n	1
M_{PASS}	32 µ	500n	10

The layout of the proposed LDO is laid out using GPDK0.90 µm CMOS technology as shown in Fig.7. Common centroid technique is implied for layout of transistors to achieve better matching. The huge pass transistor is split into 100 transistor blocks so as to minimize the chip area. The proposed LDO acquires an area of 0.0299µm^2.

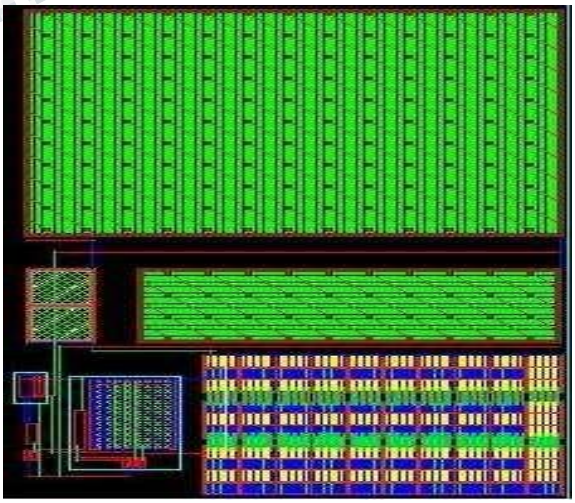

Figure 7: Top Level Layout

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IV. SIMULATION RESULTS

Simulations of the designed capacitor-less LDO is carried out using Cadence Spectre simulator in analog design environment. The simulations are divided into open loop ac response showing frequency domain analysis, transient response for line and load regulations, and PSR analysis.

Open loop ac response is shown in Fig. 8. It shows gain of 61.9175 dB with output capacitance C_{out} equal to 2.7pF and load current equal to 100 mA.

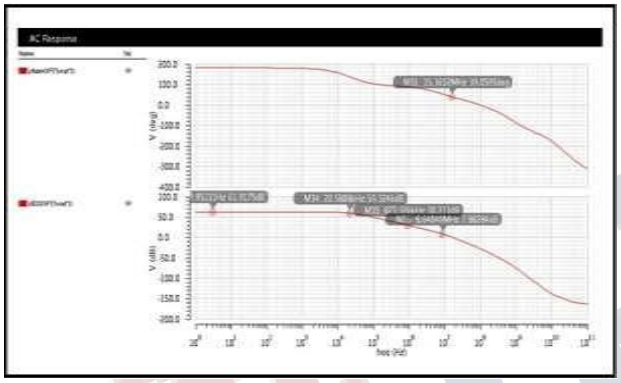

Fig 8: Open loop ac response for Iload = 100 mA and Cout = 2.7pF.

From Fig. 9 and Fig. 10, line and load regulations for Iload = 100 mA is calculated as 6.38mV/V and 0.0272mV/mA respectively. Line regulation is measured by sweeping Vin from 1.62 V to 1.98 V and load regulation is measured by varying load current from 0 A to 100 mA with a supply voltage of 1.8 V.

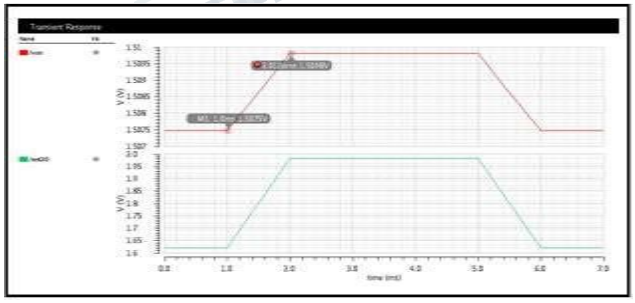

Fig 9: Line regulation at ILOAD = 100 mA.

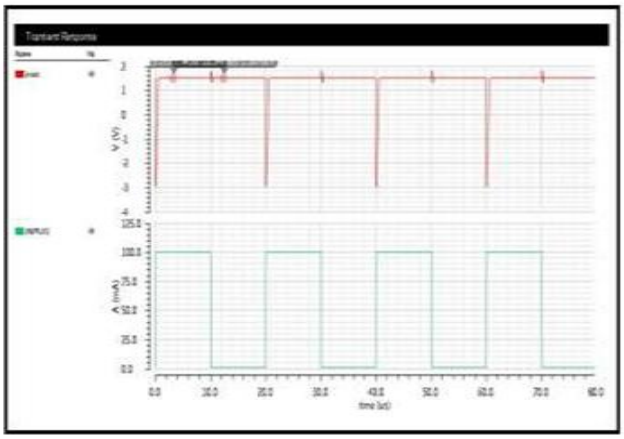

Fig 10: Load regulation at ILOAD = 100 mA.

PSRR of -43.741 dB is achieved upto 1kHz and -39.130 dB upto 1MHz for load current of 100 mA with output capacitance of 2.7 pF as shown in Fig. 11. Settling time of 0.5 µs is observed when there is a step change in input voltage of 0 V to 1.8 V.

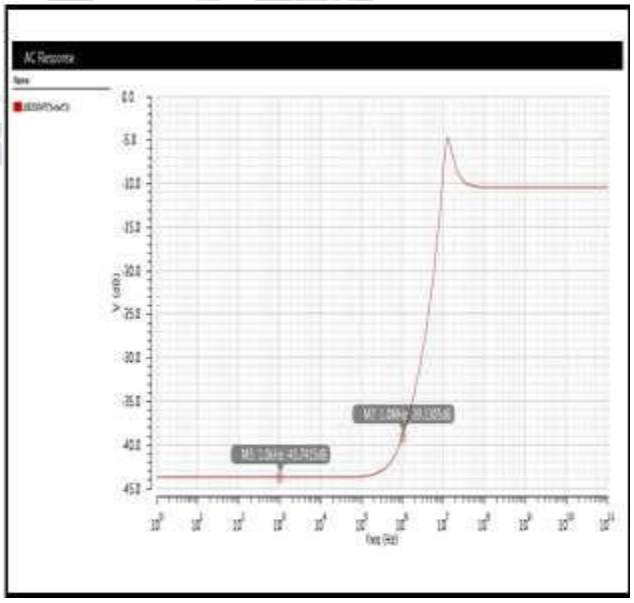

Fig 11: PSRR curve at ILOAD = 100 mA and Cout = 2.7 pF.

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Table ii : summary of the performance of the proposed Cmos ldo

DESCRIPTION	SIMULATED VALUES	UNITS
V_{IN}	1.8	V
V_{OUT}	1.5	V
V_{DROP}	300	mV
I_{MAX}	100	mA
I_Q	15.09	µA
LOAD REGULATION	100mA load: 0.027 50mA load : 0.034	mV/mA
LINE REGULATION	6.38	mV/V
PSRR	1kHz = -43.741 1MHz = -39.130	dB
AC RESPONSE	100mA load : 61.91 0mA load : 88.96	dB
SETTLING TIME	0.5	µsec
C_{out}	2.7	pF
EFFICIENCY	83.33	%
AREA	0.0299	μm^2

V. CONCLUSION

The proposed architecture for a capacitor-less LDO voltage regulator designed using GPDK 0.90 µm CMOS technology regulates the output voltage at 1.5 V from a minimum supply of 1.8 V delivering a load current upto 100mA at the output. The proposed capacitor-less topology uses a common differential amplifier and second stage amplifier which helps to fix the operating point of pass transistor stage. The proposed LDO structure is beneficial for system-on-chip designs since it helps to eliminate many off-chip capacitors while preserving high static-state, frequency, and transient performances. The simple structure and small chip area are additional advantages for on-chip local voltage regulators of integrated systems.

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