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Review on Implementation of ALU using reversible logic gates and Vedic Mathematics

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Abstract: **Arithmetic and logic unit (ALU) is a part of central processing unit that carries out arithmetic and logical operations and consists of many computational units like adders, multipliers, logic unit etc. In this review paper, ALU based on reversible logic gates and Vedic Mathematics concepts are discussed. Here reversible logic gates are used instead of the basic logic gates such as AND, OR etc which will function in the same way as that of the basic logic gates. An important requirement of digital system is to reduce power dissipation. By using reversible ALU instead of using basic logic gates power consumption is lowered. Also a high speed 8x8 bit multiplier based on Vedic multiplier mechanism is explained.**

Keywords: **ALU, FPGA, reversible logic, VedicMathematics, Xilinx ISE 14.1**

I. INTRODUCTION

Power dissipation is a limiting factor that can be reduced with the help of using reversible logic. Power dissipation in very large scale integration (VLSI) systems is very high because of the rapid switching of internal signals and also the systems designed using conventional circuits dissipate heat due to loss of information bits during computation. Energy dissipation is proportional to the number of bits lost during computation. Reversible ALU reduces the information bits and hence we can lower the power consumption. In reversible circuits, the information bits are not lost and also it can generate unique outputs from specified inputs and vice-versa.

A Vedic Mathematics is another concept that is more efficient than the conventional method for performing the various mathematical computations. The use of Vedic Mathematics concepts in computation algorithm of a processor will reduce the complexity of area, the execution time, and power consumption etc. Urdhva-Tiryakbyham is the general formula which is applicable to all the cases of multiplication and also in the division of a large number by another large number. Urdhva-Tiryakbyham Vedic method is used for eliminating unwanted multiplication steps with zeros and scaled to higher bit level and used to build high speed power efficient multiplier in a processor.

II. RELATED WORK

Landauer [1] proposed a design that showed loss of information bits results in dissipation of KT*ln2 J of heat energy where K is Boltzmann constant and T is temperature. For example the AND gate, has two inputs and one output, one bit is lost when the information bits go through this gate. For every bit of information loss, it will generate KT*ln2 joules of heat energy. Bennett [2] showed that loss of information bits can be reduced by using reversible logic circuit. Viswanath and Ponni [3] implemented using reversible logic gate and its performance was analyzed. Rahul Nimje et al. [4] proposed ALU design using Vedic Mathematics techniques. Here processor load is reduced by connecting the main processor with coprocessor which is designed to function like numeric computation, image processing and arithmetic operation. Abhishek Gupta [5] has proposed an ALU design which performs three arithmetic operations eight different logical operations at high speed. S.P.Pohoker et al. [6] proposed ALU design using Vedic Mathematics method.

Here multiplication steps are reduced which in turn reduces the propagation delay and thus reduces hardware complexity. Abhyarthana Bisoyil et al. [7] proposed an ALU design with binary multipliers, where addresses are used in the design and development of ALU. The aim of this paper was to implement digital multipliers based on the concept of Vedic Mathematics. In order to design a digital multiplier, Urdhva-Tiryakbyham sutra of Vedic
Mathematics is used.

III. THE ARITHMETIC LOGIC UNIT (ALU) BASED ON REVERSIBLE LOGIC GATES

3.1 8-Bit Adder/Subtractor

The reversible full adder/subtractor [8] is realized using Peres Gate [9] and Feynman gates [10] as shown in Figure 1,

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where Ctrl, A, B and Cin are the inputs and S/D and C/B are the outputs of the adder/subtractor unit. Addition is selected by assigning the Ctrl value as zero and the Ctrl value as 1 for subtraction. Signals g1, g2 and g3 are the garbages of the unit. The 8-bit reversible ripple carry adder/subtractor is designed by placing the adder units as shown in Figure 2.

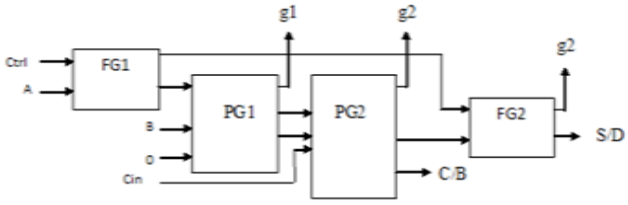

Figure 1. Reversible design of full adder/subtractor

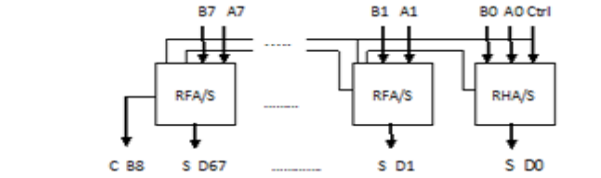

Figure 2. Design of 8-bit adder/subtractor.

3.2 8-Bit Multiplier

HNG gates [11] and Peres gate are used to perform multiplication and has two phases. In first phase partial products are generated in parallel. The output contains both partial products and garbages. In the second phase addition of partial products is done using reversible half-adder and full-adder gates constructed using the PG and HNG gate as shown in Figure 3 and the product P for inputs x and y is obtained.

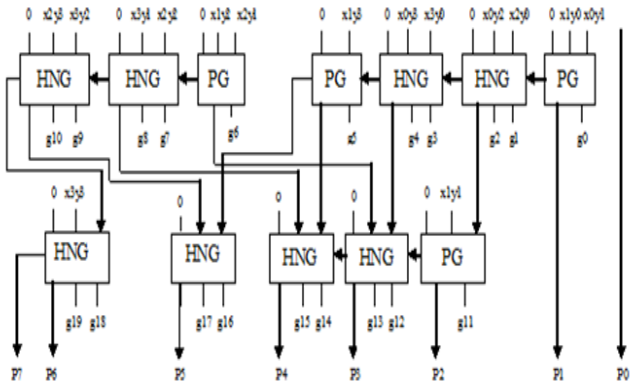

Figure 3. 8-Bit multiplication.

3.3 Logical Unit

The basic logical operations included in this unit are AND, OR, NOT, NAND, NOR, XOR. The AND and OR gates are realized using the Fredkin gate [12]. The XOR and NOT operations are realized using Feynman gate. The NAND and NOR gates are realized using the new gate.

4. The Arithmetic Logic Unit (ALU) based on Vedic Mathematics

Figure 4 shows the block diagram of Vedic Mathematics based ALU design. The latches are used to store the two binary inputs and output result of an arithmetic or logic operation. The multiplexer is used to route the result of a selected operation to the output latches.

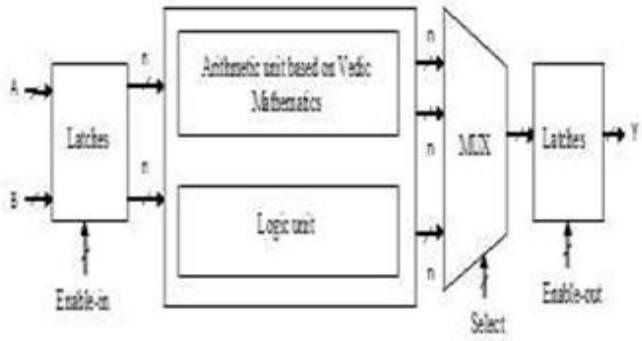

Figure 4. Block diagram of the Vedic Mathematics based ALU

Figure 5. Block diagram of arithmetic unit of the ALU

Figure 5 is the block diagram for implementation of the Vedic Mathematics based arithmetic unit of the ALU. The addition is carried out using robust adders. The multiplication is carried out by using the Urdhva-Tiryakbyham Sutra. The Urdhva-Tiryakbyham Sutra is used to construct 2x2 multiplier blocks. Several such 2x2 multipliers along with ripple carry adders are used to design 4x4 multiplier blocks. This procedure is repeated to obtain the higher order multiplier blocks. The 8-bit Vedic Mathematics based arithmetic unit of ALU includes adder, subtractor, multiplier, divider and the logic unit.

IV. CONCLUSION

Design and implementation of ALU with reversible logic gates done in high level hardware description language, synthesized using EDA tool and implemented on Xilinx Spartan-6 is presented. ALU implementation using reversible logic gates showed 39% reduction in power dissipation when compared to the implementation using basic gates. ALU implementation using Vedic Mathematics concept showed lower power dissipation as compared to ALU implemented using basic gates.

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