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Design and Implementation of Vedic Multiplier using Verilog Code on FPGA

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***Abstract* - Currently the speed of the multipliers is limited by the speed of the adders used for partial product addition. We proposed an 8-bit multiplier using a Vedic Mathematics (Urdhva Tiryagbhyam sutra) for generating the partial products. The product addition in Vedic multiplier is realized using partial products in parallel. An 8-bit multiplier is realized using a 8 and 12 bit parallel adders. In the proposed design we have reduced the number of logic levels, thus reducing the logic delay. Simulation of the architecture is synthesized using Xilinx ISE9.1.The performance of the proposed multiplier has been compared with those other multipliers reported in literature.**

***Keywords:* Vedic Mathematics, Urdhva Tiryagbhyam Sutra, Parallel Adder Technique.**

1.INTRODUCTION

Multipliers are the key components of systems viz. FIR filters, Microprocessors, Digital Signal Processors etc. which demands high performance. The performance of these applications mainly depends on the numbers of multiplication done in unit time. In real time multipliers the speed and power are the major criteria, thus faster and power efficient multipliers are needed. This paper focuses on the development of high speed, low power multipliers using Vedic Mathematics. The proposed multiplier architectures are based on the Urdhva sutra of the Vedic Mathematics. The Urdhva multiplier generates the partial products and the sums in parallel. Hence, this multiplier reduces the carry propagation delay from LSB to MSB. The proposed Urdhva multiplier achieve 60% improvement in speed and 37% improvement in power respectively, as compared with the power consumption of the conventional array multipliers.

Multipliers are the crucial arithmetic operation in DSP and general computer system because the overall performance of the system is significantly influenced by the speed of the multipliers.so it is important that the multipliers should be fast and efficient. Generally the multiplication involves two basic operation i.e generation of partial product and their accumulation. Consequently, fast multiplication can be achieved either by reducing tbe number of partial products or by accelerating the accumulation.so the requirement of fast multiplication can be achieved by using the concept of vedic mathematics using the UT(urdhva tiryagbhyam)sutra.

In the conventional vedic multipliers,the multiplication of 8x8 bit was carried out by using traditional vedic concept.i.e vertically and cross wise.In our existing system we have modified the multiplication technique. Instead of direct multiplication we have splitted 8x8 bit into four 4x4 bit and multiply them.on doing so,we were able to reduce the number of partial products and hence decrease the propagation delay.

2. PROJECT OBJECTIVES

The major objectives of our project are:

- To implement 8x8 multiplication using four 4x4 bit multipliers and hence reducing the complexity.
- To increase the computation speed using UT sutra
- To decrease the number of gates which in turn decreases the area and minimise the delay of computation.
- Due to parallel mechanism partial product are added at the same time which increases the speed of computation.

3.LITERATURE SURVEY

Urdhva Tiryagbhyam sutra which is the General Formula applicable to all cases of multiplication and will also be found very useful later

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on in the division of a large number by another large number. The formula itself is very short and consisting of only one compound word and means "vertically and cross-wise."

In ref[1] Himanshu Thapliyal, at 2009, have proposed parallel architectures for computing square and cube of a given number based on Vedic mathematics. For the Xilinx FPGA family, it is observed that for8−bit, the gate delay of the proposed square architecture is 28 ns with area of 90 while it is 70 ns for previously reported squares with area of 77. For the same operand size, the gate delay in the proposed cube architecture is 28 ns with area of 90 while for the cube previously reported is 79 ns with area of 768. As the operand width is increased to 16, the gate delay of the proposed square architecture increases slightly to 38 ns with area of 348 while for the square proposed earlier, it significantly increases to 70 ns with area of 441. For the operand size of 16, the cube statistics are found to be 54 ns with area of 1336 for the proposed Vedic cube while it is 186 ns with area of 6550 for the cube proposed before.

In ref[2],The paper presents the design of 8-bit Vedic multiplier simulated in EDA (Electronic Design Automation) tool – XilinxISE14.3 . The implementation of Vedic multiplication method results in highly compact layout leading to small contribution of interconnections to the overall propagation delay was 23.620nsec.

In paper [3] S. Deepak, et al, 2012, have proposed a new multiplier design which reduces the number of partial products by 25 %. This multiplier has reported to have been used with different adders available in literature to implement multiplier accumulator (MAC) unit and parameters such as propagation delay, power consumed and area occupied have been compared in each case. The results obtained have been compared with that of other multipliers and it has been reported that the proposed multiplier has the lower propagation delay when compared with Array and Booth multipliers.

In paper [4] A high speed complex multiplier design (ASIC) using Vedic Mathematics has also been reported by Prabir Soha, et al, 2011. A complex number multiplier design based on the formulas of the ancient Indian Vedic Mathematics, was said to have been implemented in Spice spectra and compared with the mostly used architecture like distributed arithmetic, parallel adder based implementation, and algebraic transformation based implementation. The proposed complex number multiplier has been reported to offer 20% and 19% improvement in terms of propagation delay and power consumption respectively, in comparison with parallel adder based implementation.

This is the conventional hardware architecture of vedic multiplier where the speed, delay, power consumption is high which is shown below in Fig 1.

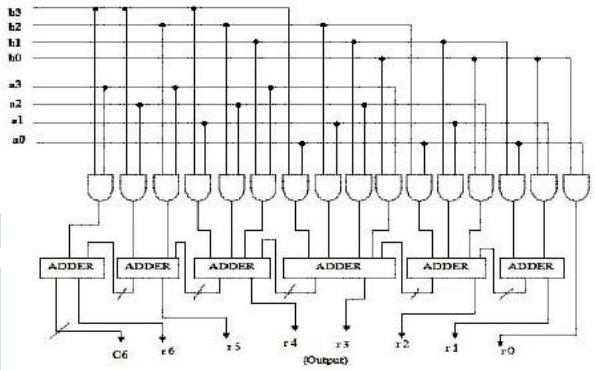

Fig 1. UT Multiplier Conventional Hardware Architecture

4. VEDIC MATHEMATICS

The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. Vedic Mathematics introduces the wonderful applications to Arithmetical computations ,theory of numbers, compound multiplications, algebraic operations, factorizations, simple quadratic and higher order equations, simultaneous quadratic equations, partial fractions, calculus, squaring, cubing, square root, cube root, coordinate geometry and wonderful Vedic Numerical code.

5. URDHVA TRIYAGBHYAM SUTRA

'Urdhva' and 'Tiryagbhyam' words are derived from Sanskrit literature. 'Urdhva' means 'Vertically' and 'Tiryagbhyam' means 'Crosswise'. It is based on a novel

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concept through which the generation of all partial products can be done with the concurrent addition of these partial product. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line is there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other

In the binary system only 0 and 1 are used hence multiplication in Urdhva Tiryagbhyam or vertically-crosswise formula is replaced by AND logic. AND logic is performed between two binary numbers for multiplication and addition is done according to binary logic. Let us consider the multiplication of two binary numbers A3A2A1A0 and B3B2B1B0 with carry C6C5C4C3C2C1C0. As the result of this multiplication would be more than 8-bit we express it as the below expressions: -

R0 = A0B0

R1 = A0B1+B1A1+C0

bits act as carry for the next step. Initially the carry is taken to be zero.

6. MULTIPLIER ARCHITECTURE

- The multiplier is based on an algorithm Urdhva Tiryagbhyam(vertical & crosswise).
- This sutra shows how to handle multiplication of larger number (NxN bits) by breaking it into smaller sizes.
- For multiplier, first the basic blocks, that 2x2 multiplier are made and then 4x4 block ,8x8 block have been made.
- The device selected for synthesis is Device family Spartan 3E.

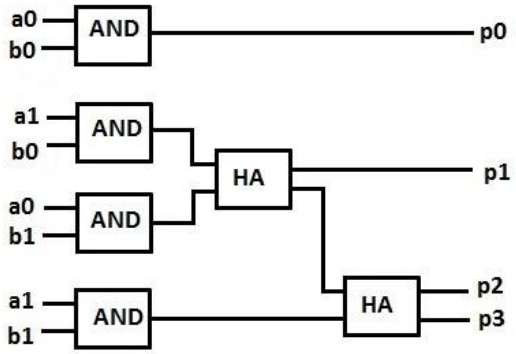

Fig 2. Basic 2-bit Multiplier Architecture

7. BINARY MULTIPLICATION URDHVATRIYAGBHYAM

R2 = A2B0+B2A0+A1B1+C1

R3 = B0A3+B3A0+A2B1+B2A1+C2

R4 = A3B1+A1B3+A2B2+C3

R5 = A3B2+B3A2+C4

R6 = A3B3+C5

R7 = C6

ALGORITHM

Let us consider the algorithm for 4x4 bit multiplication. To illustrate the multiplication algorithm, let us consider the multiplication of two binary numbers A3A2A1A0 and B3B2B1B0. As the result of this multiplication would be more than 4 bits, we express it as... R3R2R1R0. Line diagram for multiplication of two 4-bit numbers is shown in Fig 3 which is nothing but the mapping in binary system. For the simplicity, each bits represented by a circle. Least significant bit R0 is obtained by multiplying the least significant bits of the multiplicand and the multiplier.

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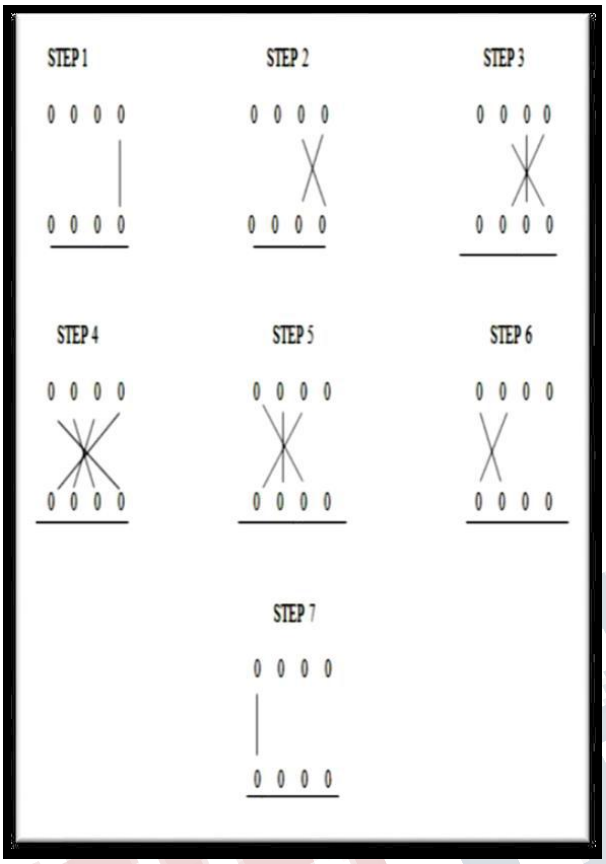

Fig 3. Line diagram for multiplication of two 4- bit number

Line diagram for multiplication of two 4-bit numbers is shown in Fig 3. Firstly, least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits of the two numbers from least significant position.

8. COMPARISON AND RESULT

The comparison between Vedic multiplier by Urdhva Tiryagbhyam and conventional multiplier is made. The Vedic multiplier is smallest and the fastest of the reviewed architectures. Due to its parallel and the regular structure, this architecture can be easily realised on silicon and can work at high speed without increasing the clock frequency. It has advantage that as the number of bits increases, the gate delay and the area increases very slowly as compared to other multiplier architectures. Speed improvements are gained by parallelizing the generation of partial products with their concurrent summations.

Table 1 shows the comparison between the proposed multiplier with Wallace multiplier and Multiplier using normal gates. Here the proposed multiplier shows the less delay then the other multiplier

Table 1. Comparison between the multiplier

Device: Spartan	Wallace Tree (ns)	UT (ns)	UT (ns)
XC3S100E-5TQ144	Multiplier	Multiplier using Normal Gates	Proposed Multiplier
Path Delay	25.712	23.620	19.375

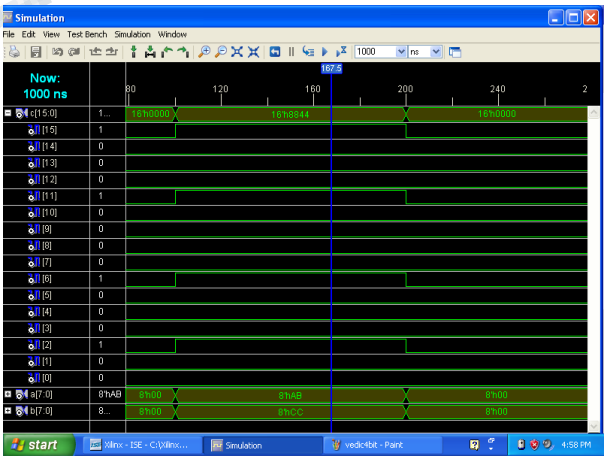

Fig 4. Simulation for 8-bit Vedic Multiplier

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This is the testbench waveform of 8-bit vedic multiplier. This is one of the example of eight bit multiplier.

A=10101010

B=11001100

Result=1000100001000100

9. CONCLUSION

This paper presents a highly efficient method of multiplication – "Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. It gives us method for hierarchical multiplier design and clearly indicates the computational advantages offered by Vedic methods. The computational path delay for proposed 8x8 bit UT multiplier using parallel adder is found to be 19.375 ns. Hence our motivation to reduce delay is finely fulfilled.

10. REFERENCES

- Ref [1] Himanshu Thapliyal, Saurabh Kotiyal* and M.B Srinivas, Design and Analysis of A Novel Parallel Square and Cube Architecture Based On Ancient Indian Vedic Mathematics.
- Ref [2] Design Of A High Speed 8x8 Ut Multiplier Using Reversible Logic Gates Sadhu Suneel1, L.M.L.Narayana Reddy M. Tech student , Assistant professor in ECE department.
- Ref [3] S. Deepak and Binsu J Kailath, 2012, Optimized MAC unit design, (2012) IEEE EDSSC 2012, IEEE International Conference on Electron Devices and Solid-State Circuits held from 3-5 Dec. 2012.
- Ref [4] Prabir Saha, Arindam Banerjee, Partha Bhattacharyya , Anup Dandapat, 2011. High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics, IEEE Students' Technology Symposium, IIT Kharagpur.
- Ref [5] Ramachandran.S, Kirti.S.Pande, Design, Implementation and Performance Analysis of an Integrated Vedic Multiplier Architecture, International Journal Of Computational Engineering Research, May-June 2012, Vol. 2. Issue No.3, 697-703.
- Ref [6] Pavan Kumar U.C.S, Saiprasad Goud A, A.Radhika, FPGA Implementation of High Speed 8-bit Vedic Multiplier Using Barrel Shifter, International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 3, March 2013.
- Ref [7] Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho, Multiplier design based on ancient Indian Vedic Mathematics, 2008 IEEE International SOC Design Conference.
- Ref [8] Vinay Kumar, 2009 Analysis, Verification and FPGA Implementation Of Vedic Multiplier With Bist Capability, Thapar University.