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Different Memristive Functions For Implementing Memristor Spice Model

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Abstract: **-- Memristor is a novel two-port circuit element with a memory, as device that can be used in many applications such as memory, logic, and neuromorphic systems. As passive circuit element the memristor would be a useful tool to analysis circuit behavior via simulation. SPICE model is appropriate way to describe real device operation. In this paper, we incorporate a SPICE model of memristor with threshold logic circuit for nonlinear dopant drift. Various window functions has been proposed in nonlinear ion drift memristor devices. Circuit analysis of the proposed memristor models are studied by investigating and characterizing the physical electronic and behavioral properties of memristor device. The simulation output should have a current–voltage hysteresis curve, which looks like bow tie. The loop maps the switching behavior of the device. Then, make comparison of these memristor implemented circuit design between different type of memristor window models. The research verifies the proposed threshold memristor model and the possibilities of implementing memristor model in practical analog circuit.**

Keywords:-- **memristor, memristor SPICE model, non linear, window functions.**

I. INTRODUCTION

Memristor is the contraction of memory resistor which is a passive device that provides a functional relation between charge and flux. It is defined as a two-terminal circuit element in which the flux between the two terminals is a function of the amount of electric charge that has passed through the device [1]. A memristor is said to be charge-controlled if the relation between flux and charge is expressed as a function of electric charge and it is said to be flux-controlled if the relation between flux and charge is expressed as a function of the flux linkage [2].

Low-power high -density memory devices are critical to a very wide range of integrated applications. With IC technology scaling, there exists a great interest in searching for the next generation of universal memories, which are able to ubiquitously replace traditional SRAM, DRAM and nonvolatile memories such as flash memory. Very recently, a new device with pinched hysteresis was demonstrated [2], which was recognized as the first real-life realization of the so-called missing fourth circuit element, memristor, whose existence was theoretically predicted by L. Chua in 1971. Leon Chua proposed that there should be a fourth fundamental passive circuit element to set up a mathematical relationship between electric charge and magnetic flux which he called the memristor which is short for memory resistor [2].

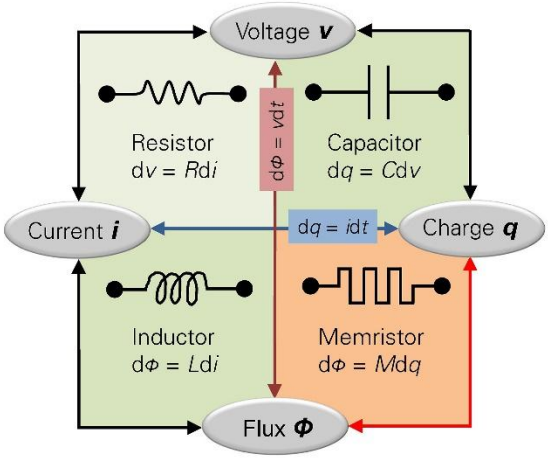

Figure 1: Relationship between fundamental circuit element

The current is defined as the time derivative of the charge. According to Faraday‘s law, the voltage is defined as the time derivative of the flux. A resistor is defined by the relationship between voltage and current dv=Rdi, the capacitor is defined by the relationship between charge and voltage dq=Cdv, the inductor is defined by the relationship between flux and current dφ=Ldi. The fourth fundamental circuit element completes the symmetry of the relation between charge and magnetic flux dφ=Mdq. figure 1 show the

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relationship between the fundamental circuit element.

The memristor has a memristance and provides a functional relation between charge and flux. In 2008, Stanley Williams and his team at Hewlett Packard successfully fabricated the first memristor in physical device form [3]. Memristance is a property of the memristor. When the charge flows in one direction through a circuit, the resistances of the memristor increase. The resistance decreases when the charge flows in the opposite direction in the circuit. If the applied voltage is turned off, thus stopping the flow of charge, the memristor remembers the last resistance that it had [1].

In HP memristor model, to realize a memristor, they used a very thin film of titanium dioxide (TiO2). The thin film is sandwiched between two platinum (Pt) contacts and one side of TiO2 is doped with oxygen vacancies. The oxygen vacancies are positively charged ion and make it conductive. Thus it behaves as semiconductor. There is a TiO2 junction where one side is undoped. The undoped region has insulating properties. The device established by HP is shown in Figure 2 [3].

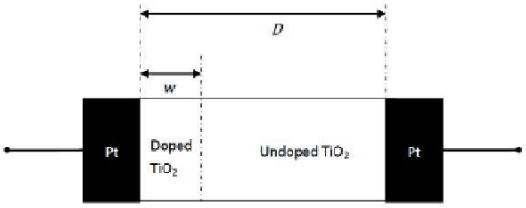

Figure 2: Memristor model adapt from [3].

When a positive voltage is applied, the positively charged oxygen vacancies in the TiO2-x layer are repelled and moving them towards to the undoped TiO2 layer. The boundary between the two materials moves causing an increasing in the percentage of the conducting TiO2-x layer and thus increasing the conductivity of the whole device.

When a negative voltage is applied, the positively charged oxygen vacancies are attracted and pulling them out of TiO2 layer. This increases the amount of insulating TiO2, thus increasing the resistivity of the whole device. When the voltage is turned off, the oxygen vacancies do not move. The boundary between the two titanium dioxide layers is frozen. This is how the memristor remembers the voltage last applied [1].

II. METHODOLOGY

Our aim in this project is to provide a simulation program adequately simulates and can be used as a circuit element in design work. To model the electrical characteristics of the memristors, SPICE would be appropriate way to describe real device operation [4]. Moreover, using the model as a sub-circuit can highly guarantee a reasonable high flexibility and scalability features [5].

We use PSPICE to create a memristor model and design new symbol of the memristor circuit for the simulation because PSPICE is much easier to handle compared to others. We use SPICE model that been adapt from [6] and made some adjustment so we can use it for several of window function that has been proposed for non linear ion drift model.

The SPICE model is created based on the mathematical model of the HP Labs memristor. After the memristor has been modeled, then we will start to design and implement the memristor with an analog circuit. We will investigate and made a comparison between the memristor circuit with analog circuit to see the difference and study the behavior of the circuits.

Model of the memristor from HP Labs

In the model of a memristor presented here, there is a thin semiconductor film that has two regions, one with a high concentration of dopant that behaves like a low resistance called RON and the other with a low dopant concentration with higher resistance called ROFF [3]. The film is

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sandwiched between two metal contacts as in figure 2.

The total resistance of the memristor, RMEM, is a sum of the resistances of the doped and undoped regions, is the width of the doped region, referenced to the total length D of the TiO2 layer, and ROFF and RON are the limit values of the memristor resistance for w=0 and w=D. The ratio of the two resistances is usually given as 102 - 103.

$$R_{MEM}(x) = \left(R_{ON}(\mathrm{x}) + R_{OFF}(1-x)\right) \quad (1)$$

Where $x = \frac{w}{D}\ \epsilon(0,1)$ (2)

The Ohm's law relation is applicable between the memristor voltages and current

$$v(t) = R_{MEM}(w)i(t) \quad (3)$$

The application of an external bias v(t) across the device will move the boundary between the two regions by causing the charged dopants to drift. For the simplest case of ohmic electronic conduction and linear ionic drift in a uniform field with average ion mobility μv, we obtain

$$v(t) = (R_{ON}\frac{w(t)}{D} + R_{OFF}(1-\frac{w(t)}{D}))i(t) \quad (4)$$

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{D} i(t) \quad (5)$$

Which yields the following formula for w(t)

$$w(t) = \mu_v \frac{R_{ON}}{D} q(t) \quad (6)$$

By inserting equation (6) into equation (4) we obtain the memristance of this system, which for RON=ROFF simplifies to

$$M(q) = R_{OFF}(1 - \frac{\mu_v R_{ON}}{D^2} q(t)) \quad (7)$$

Where μv is the average drift velocity(cm2/Sv), D is the thickness of titanium-dioxide film ROFF and RON are on-state and off-state resistances and q(t) is the total charge passing through the memristor device. when voltage is 1V, memristor is switching from ROFF (undoped) to RON (doped) region happen whereas when voltage is -1V, memristor is switching from doped to undoped region. At this switching point, x is at middle position (w/D=0.5 when voltage is 1V and -1V). Meanwhile, the highest resistance and lowest resistance are both achieved at 0V. whenever voltage is 0V, x is at outmost position (0 or 1). Here, memristor is switching when voltage is 1V and -1V where the boundary position is at middle. The amount of voltage to push boundary from middle to either doped/undoped region to allow device switching is called the threshold voltage. Any voltage below threshold voltage only change the resistance value, but not able to switch on/off the device.

As explained before, w denotes the length of doped region whereas x indicates boundary between doped and undoped region. When x is larger, doped area ratio is increased thus resistance becomes lower. The structure of memristor during particular voltage points is explained in Figure 2 based on boundary position at Figure 3. When voltage increase from 0V to 1V in (a), the positively charged dopants in the doped TiO2- x layer are repelled, moving them towards the undoped TiO2 layer. As a result, the boundary between two materials shifts, causing an increase in the percentage of the conducting TiO2-x layer. This increases the conductivity of the whole device. When voltage decreases from 1V to 0V in (b), the charged dopants still moving, but with slower speed and resistance decreases steadily. When a negative voltage increase from 0V to -1V in (c), charged dopants are attracted, pulling them out of TiO2 layer. This increases the area of undoped TiO2 layer thus increasing the resistivity of the whole device. When voltage changes from -1V to 0V in (d), the charged dopants still moving, but with slower speed and resistance increases steadily.

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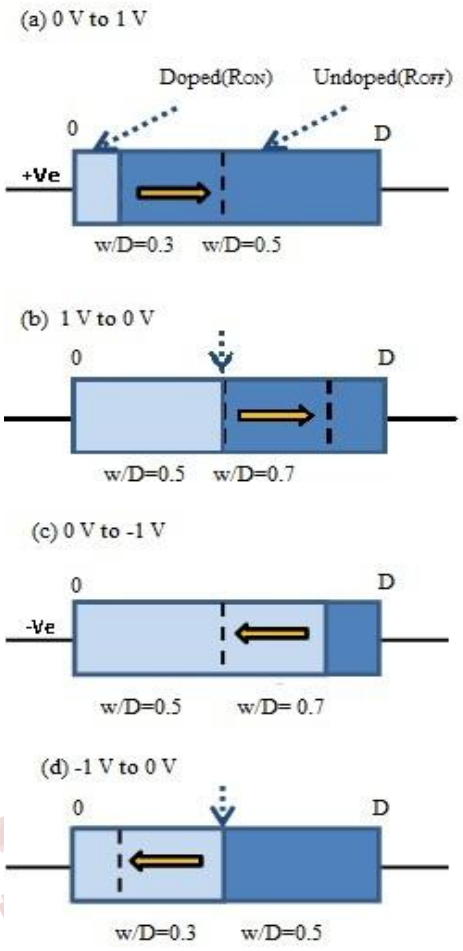

Figure 3: Boundary position, x at few voltage point

Non linear ion drift model

Even a small voltage across the nano devices will produce a large electric field [7]. This causing the ion boundary position will move in a decidedly non-linear. Nonlinear dopant drift adds nonlinear window function f(x) to the state equation within zero and unity. The window function decreases as the state variables drift speed approaches the boundaries until it reaches zero when reaching either boundaries [8]. The speeds of the movement of the boundary between the doped and undoped regions are depending on several factors according to state equation [1]

$$\frac{dx}{dt} = ki(t)f(x), \qquad k = \frac{\mu_v R_{ON}}{D^2} \quad (8)$$

Where uv is the dopant mobility. The speed of the boundary between the doped and undoped regions decreases gradually to zero [1]. We simulate the nonlinear ion drift memristor model with these window function to see the difference and the issue that been faced by them. When you submit your final version, after your paper has been accepted, prepare it in two-column format, including figures and tables.

III. WINDOW FUNCTIONS

`Window function is a function of the state variable. Window function forces the bounds of the device and to add nonlinear behavior close to these bounds. There are several window functions that have been proposed till date. We implemented these window function in the SPICE model to see the difference and the issue that been faced by them. The implemented window functions are: Strukov, Joglekar and Wolf, Biolek, and Prodromakis.

Several window functions were proposed in the literature. Strukov proposed the following window function [3]

$$f(x) = x - x^2 \quad (9)$$

However, this window function lacks of flexibility. Another window function was proposed by Joglekar [4], which has a control parameter p which is a positive integer.

$$f(x) = 1 - (2x - 1)^{2p} \quad (10)$$

This control parameter controls the linearity of the model, where it becomes more linear as p increases. This window function ensures zero drift at the boundaries. However, a significant liability of this model lies in the fact that if w hits any of the boundaries (w = 0 or w = D) the state of the device cannot be further adjusted. This will be from now on termed as the terminal state problem. Until Biolek proposed another window function

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that allows the memristor to come back from the terminal state problem.

$$f(x) = 1 - (x - stp(-i))^{2p} \qquad (11)$$

The reversed bias is now should move back the state variable after it reaches either boundary. This feature is described by a current dependent step function, stp(i), which is a part of a new window function f(x) that behaves differently in each voltage bias direction.

$$stp(i) = \begin{cases} 1 & pro \quad i \geq 0 \\ 0 & pro \quad i < 0 \end{cases} \qquad (12)$$

The latest window function is proposed by Prodromakis

$$f(x) = 1 - [(x - 0.5)^2 + 0.75]^p \qquad (13)$$

It allows the window function to scale upwards which implies that fmax(x) can take any value within 0 < fmax(x) < 1. In addition, p can take any positive real number allowing a greater extent of flexibility. The boundary issues are also resolved with the window function returning a zero-value at the active bi-layer edges.

Spice model of memristor

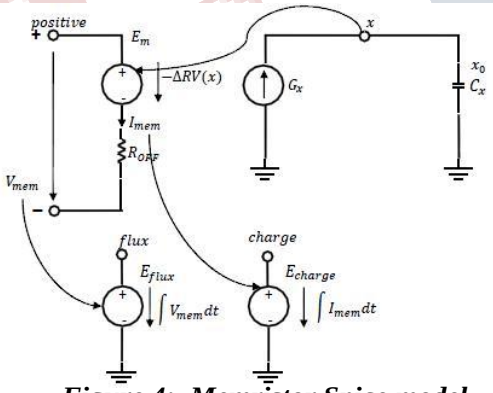

Figure 4: Memristor Spice model

In the above circuit in figure 4, VMEM is the input voltage and Imem is modeled to be the current through the memristor. The flux is calculated by integrating the voltage VMEM and the charge is calculated by integrating the current IMEM. EM is the voltage source whose terminal voltage is controlled according to the formula -xΔR. GX is a current source whose current is controlled according to the equation IMEMf(V(x)) where V(x) is the voltage across the capacitor Cx and it models the normalized width of the doped layer [6].

The relation between memristor current and voltage is modeled as on the basis of RMEM (x) = ROFF -xΔR where ΔR= ROFF-RON. ROFF is the resistor in series voltage source whose terminal voltage is controlled by the formula xΔR. The voltage V(x) across the capacitor CX models the normalized width x of the doped layer. The initial state of x is modeled by the initial voltage of the capacitor. The flux is calculated by the time-integral of voltage, and the charge is calculated by the time-integral of current.

IV. RESULTS AND DISCUSSIONS

All models were simulated in PSPICE using SPICE model that was given in [6], we add new nonlinear window functions that was proposed by prodromakis and strukov to compare all suggested window functions. Figure 5 shows a single memristor for measuring the behavior of memristor model in PSPICE with a sine wave input voltage of 1.2V with 1Hz frequency. The values for the memristor parameters uv, D, RON, ROFF and RINITIAL are 10-10cm2s-1V-1, 10 nm, 100ohm, 16kohm and 11Kohm. All model are using same window function para meter p=10.

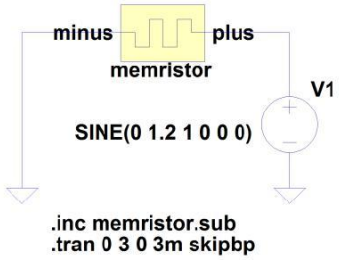

Figure 5: Memristor circuit.

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Figure 5 shows the simulation result of memristor SPICE model for Strukov window function. The figure show the I-V characteristic of the devices. The current of the memristor, IMEM for is varying up to approximately 100µA for maximum of 1.2V voltage applied. The RMEM for this model show that the values are in range of 11kOhm till 12kohm which means the effect of the volt ge applied to the memristor only give slightly changes on the value of the memristor.

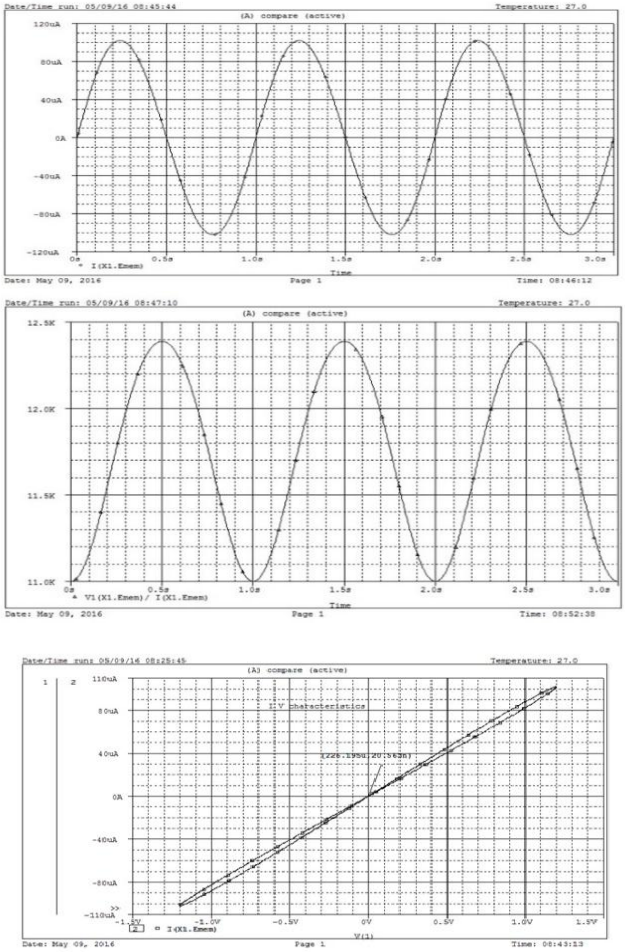

Figure 6: Strukov memristor model.

Joglekar window function seems to be promising. Figure 6 shows the simulation result of memristor SPICE model for Joglekar window function. The current of the memristor, IMEM is varying up to approximately 300µA for maximum of 1.2V voltage applied. Joglekar window function give higher current compared to others. It's show that the current in the memristor much are easier to move. The RMEM are within range of nearly 0ohm to 11kohm which give full range of value for the memristor. This shows that the value of memristor is varying when the voltage is applied thru time. The hysteresis loop I -V characteristic shows the switching behavior much more sensitive on the voltage level than Strukov window function.

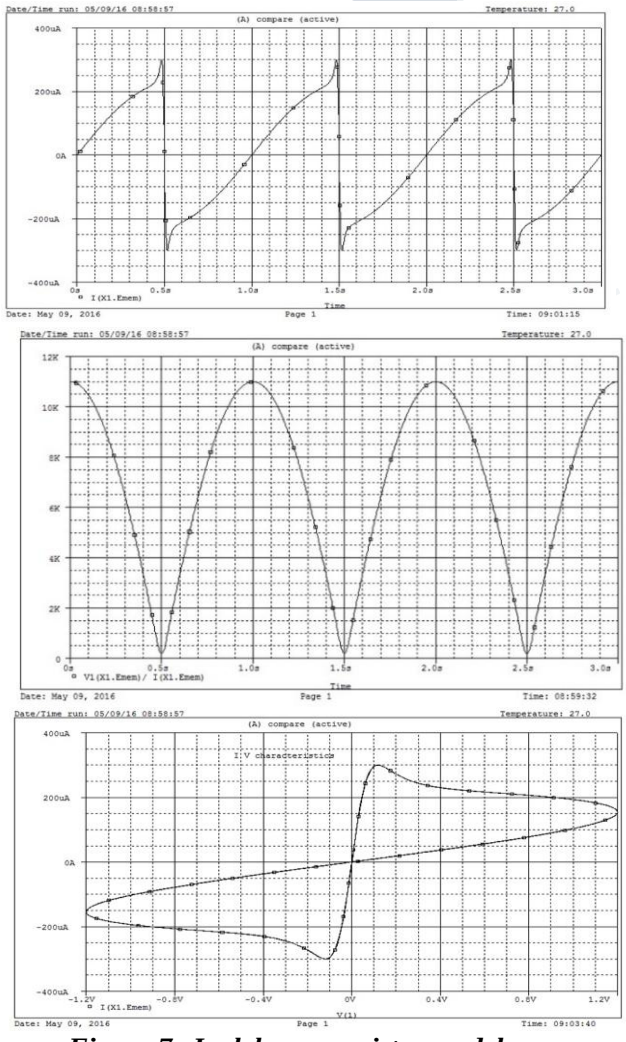

Figure 7: Joglekar memristor model.

Biolek window functions are supposed to solve terminal state problem as in literature [4]. It should

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solve the boundary problem of the terminal state. Figure 7 shows the simulation result of memristor SPICE model for Biolek window function. The current of the memristor, IMEM is varying up to approximately 220µA for maximum of 1.2V voltage applied. The RMEM are within range of nearly 1kohm to 11kohm.

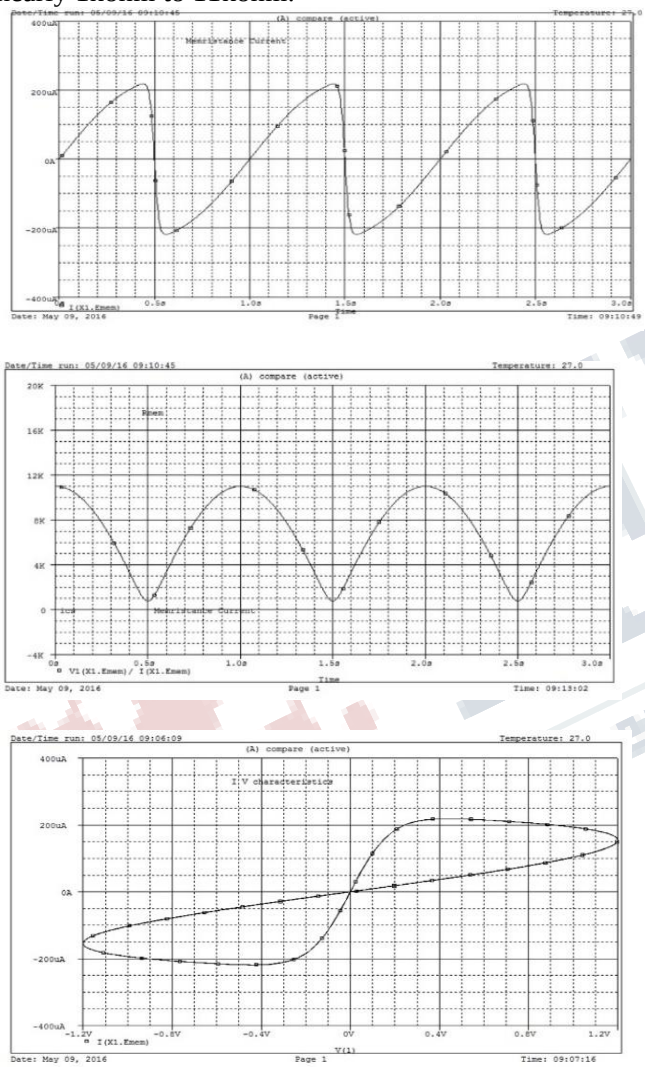

Figure 8: Biole k memristor model.

Prodromakis wind ow functions are also said to solve the boundary issue. Figure 8 shows the simulation result of memristor SPICE model for Prodromakis window function. The current of the memristor, IMEM is varying up to approximately nearly 180µA for maximum of 1.2V voltage applied. The RMEM are within range of nearly 3kohm to 11kohm. The hysteresis loop is shown to be asymmetrical while the OFF state of the device is highly non-linear compared with other.

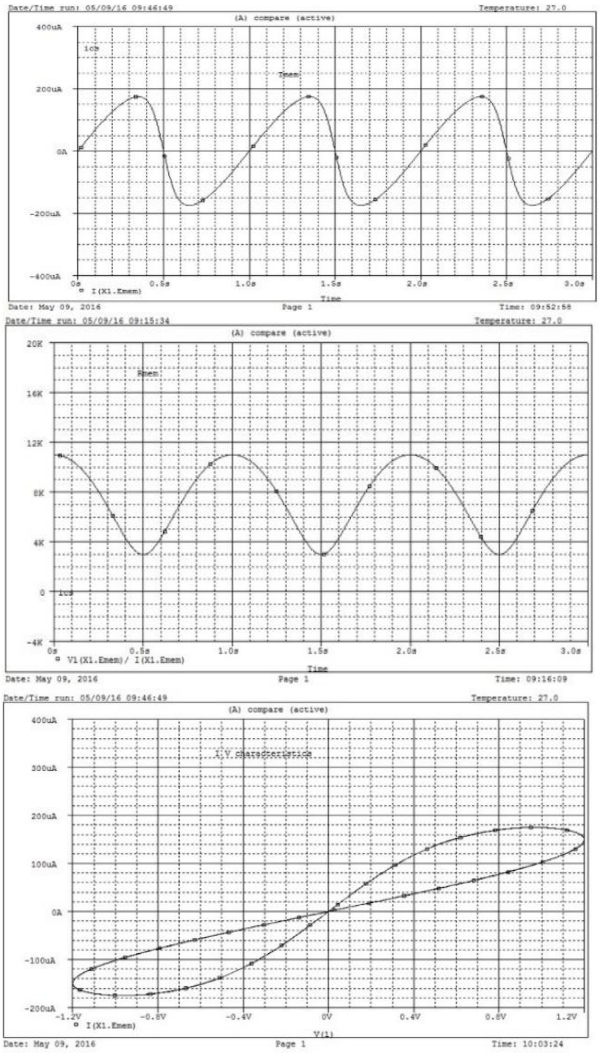

Figure 9: Prodromakis memristor model.

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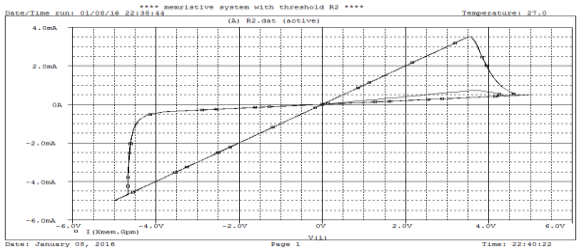

Figure 10: threshold memristor model.

In this model the current-voltage relationship is undefined and can be freely chosen from any current-voltage relationship, The dependence of the internal state derivative on current and the state variable itself can be modeled as independently multiplying two independent functions; one function depends on the state variable and the other function depends on the current.

In comparing of I-V characteristic hysteresis loop, as we can see in figure 11, it shows all hysteresis loops for all proposed window functions. By using same parameter we can see the difference in each model. Joglekar window function seems to have a strong memristance compared to others. All models seem to be a good approximation of the measurement of the real memristor produce by HP Labs.

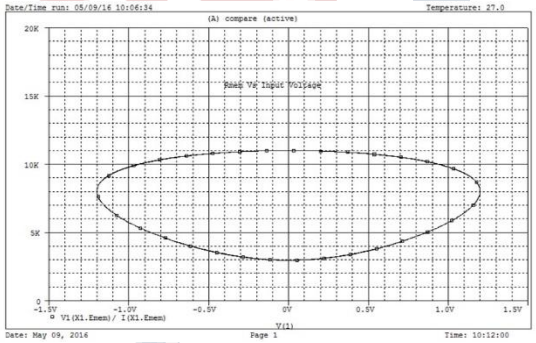

Figure 11: I-V Hysteresis Loop for all models.

V. CONCLUSION

As a conclusion to this research is that it could bring a new light of familiarization in the integration of memristive components in any kinds of electronic devices that are at nanoscale. It is useful to have a computer model of the memristor as a tool for the analysis of the behavior of the circuits in developing application of this memristor as passive circuit element via simulation. SPICE model will definitely help us to conduct interesting simulation experiments and can be of great importance for such a research in future while the memristor are still hard to fabricate to study the behavior of the circuit. Different models with strong behavior and reason give a lot of benefits in development purpose to create the possibilities of the implementation in an integrated circuit. The possibilities for implementation of the memristor with practical analog circuit are wide open.

REFERENCES

[1] R. Stanley Williams. "How we found the missing memristor", IEEE Spectrum 12.08 December 2008..

[2] L. O. Chua, (1971). "Memristor – the missing circuit element", IEEE Transactions on Circuit Theory, 18(5): 507–519.

[3] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, (2008). "The missing memristor found", Nature, 453(7191):80–83, 2008.

[4] Rak, A.; Cserey, G. "Macromodeling of the Memristor in SPICE." Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions, vol.29, no.4, pp.632-636, April 2010.

[5] Abdalla, H.; Pickett, M.D. "SPICE modeling of memristors," Circuits and Systems (ISCAS), 2011 IEEE International Symposium, vol., no.28, pp.1832-1835, 15-18 May 2011

[6] Z. Biolek, D. Biolek, and V. Biolkov´a. "SPICE model of memristor with nonlinear dopant drift", Radioengineering J. , 18(2):211, 2009b.

[7] J. Joshua Yang, Matthew D. Pickett, Xuema Li, Douglas A. A. Ohlberg, Duncan R. Stewart* And R. Stanley Williams k. "Memristive Switching Mechanism For Metal/Oxide/Metal Nanodevices" 15 June 2008; doi:10.1038/nnano.2008.160.

[8] T. Prodromakis, B. P. Peh, C. Papavassiliou, and C. Toumazou, (2001). "A versatile memristor model with nonlinear dopant

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kinetics", IEEE Trans. on Electron Devices, vol. 58, no.9, pp. 3099-3105, Sept. 2011.

[9] WILLIAMS, R. S. "How we found the missing memristor", IEEE Spectrum, 2/01/2008, p. 1-11, www.spectrum.ieee.org/print/7024.

[10] A. J. van de Goor (1998). "Testing Semiconductors Memories, Theory and Practice", John Wiley & Sons Inc.

[11] The International Technology Roadmap for Semiconductor 2011. Available online http://www.itrs.net

[12] S. Benderli and T. Wey, "On SPICE macromodelling of TiO2 memristors," Electronics letters, vol. 45, no. 7, pp. 377–379, 2009.

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