ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 3, March 2017

Design Aspects of MAP Turbo Decoder for Wireless Communication Systems

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***Abstract*— Long Term Evolution-Advanced (LTE-A) targets the peak data rates in surplus of 3Gbps for present and next generation wireless communication systems. Turbo coding, the stated channel coding scheme in 3rd Generation Partnership Project (3GPP) LTE standard, is an advanced forward error correction (FEC) coding to achieve higher throughput of advanced Wireless Communication Systems. To support the peak throughputs, parallel turbo decoding procedure has become a necessity and the corresponding VLSI implementation is extremely challenging task to the design engineers. The higher throughput applications require higher parallelism of turbo decoder design; which results in increased hardware complexity, major source of power consumption and silicon area. This paper addresses the design and implementation aspects of different parallel turbo decoders, which meet peak data rates of 3GPP LTE and LTE-Advanced standards, where throughput, power consumption, silicon area and latency are the most decisive cost factors.**

***Keywords*—3GPP, 4G LTE-A Wireless Communications, Turbo codes, Parallel Turbo decoder, VLSI.**

I. INTRODUCTION

Channel coding plays a vital role in the modern wireless communication system that deals with error control techniques to enhance the reliability of the data over a highly dispersive channel. In today's state-of-the-art iterative channel codes such as Turbo, Low-density parity check (LDPC) and polar codes achieve the high diversity, reliable data transmission and possible large coding gain in fading channels. Turbo codes were introduced by Berrou, Glavieux, and Thitimajashima [1] in 1993, capable of providing reliable communication at near-optimal transmission throughputs. Turbo coding is such a high-performance forward error correcting coding scheme designed to get BER performance within 1dB of the channel capacity [2]. By the invention of turbo coding scheme, a sudden revolution has happened in the last two decades, therefore, there was a jump from 2G system to 3G and then 4G(LTE & LTE-A) systems. Now the jump from 4G to 5G is expected with new challenges and contributions in wireless communications, which utilizes the merits of satellite communication systems.

The 3GPP LTE-Advanced standard specified by the International Telecommunication Union Radio-Communication Sector (ITUR) for International Telecommunications Advanced (IMT-A) is cited as fourth generation (4G) [10]. Turbo codes have been widely adopted in 3G and 4G wireless communication standards due to its reliable transmission and excellent forward error correction capability. The present 4G communication system (LTE/LTE-A) offer highest possible throughput up to 1Gbps (LTE-A) and excess of 1Gbps as shown in Fig. 1, by making use of Turbo codes, especially, in length code words, their performance reaches close to the maximum theoretical limits. Turbo codes find application in IEEE 802.16(Wi-MAX) 3G and 4G mobile standards such as in HSPA+, EV-DO, LTE, also in deep space satellite systems such as DVB-RCS, DVB-RCS2[11].

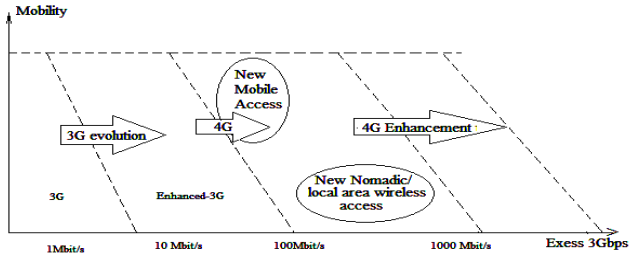

Fig. 1 Capabilities of 3G and 4G communication Systems

Turbo codes offer flexible design properties like low complexity encoder, adaptable code rate, and iterative decoding process. Decoding plays a critical role in the receiver while extracting the transmitted binary data via a noisy channel. To achieve low bit error rate (BER) and higher throughputs of 3GPP LTE-A standards, distinct

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 3, March 2017

turbo decoding algorithms have been proposed [26-28] and were directed at parallel turbo decoder architectures to achieve high throughputs.

The research is rapidly going on the design of efficient Turbo decoders and their VLSI implementations for higher throughput beyond 3Gbps for next generation communication systems. As well, the forthcoming 5th generation (5G) communication system, which is a combined system of cellular networks providing higher order data rates and satellites covering a large area. The expected achievement with the 5G system is high spectral efficiency, low battery consumption, low latency and a large number of services with very high throughput and capacity [12]. The speed performance of 5G will be more than 10 times greater than 4G Systems with high spectral efficiency. To achieve these expectations, the modulation scheme and error correcting codes able to promise very low error rates are essential. The important design parameters in 5G systems to be considered are bandwidth, energy consumption, implementation complexity and latency.

The remainder of this paper is commenced as follows. In section II, an overview of Turbo Coding of 3GPP LTE standard and various algorithm aspects of turbo decoding. Section III considers design perspective of distinct methods proposed for performance improvement is presented. Finally, Section IV summarizes the performance of various benchmark VLSI architectures of the turbo decoder. Section V concludes and future work of further decoding implementations.

II.TURBO CODING

A.Turbo Encoder

3GPP LTE standard turbo encoder is a parallel concatenation of convolutional encoders connected via an interleaver (π) as shown in LHS part of Fig.2 to encode the information bits, to be transmitted [10]. The upper encoder processes the input bits in their original order while the lower encoder processes the reordered form of the same bits. The reordered bits are produced by an interleaver π based on the quadratic permutation polynomial law defined in the LTE standards. At the output, turbo encoder generates a systematic bit sequence, non-interleaved, and interleaved parity bits.

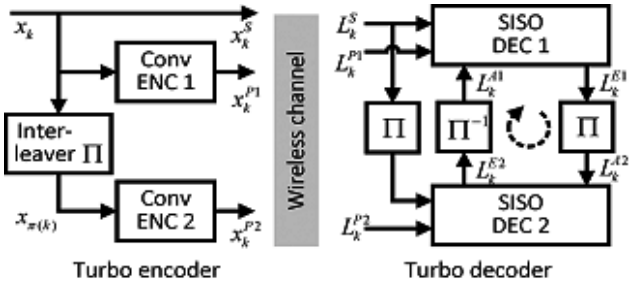

Fig. 2 Block diagram of turbo encoder and a turbo decoder.

The bits input to the Turbo code internal interleaver π are denoted by $X^S_0, X^S_1 \ldots X^S_{K-1}$, where *K* is the number of input bits.

The bits output from the Turbo code internal interleaver are denoted by $X^{P2}_0, X^{P2}_1 \ldots X^{P2}_{K-1}$.

The relationship between the input and output bits is:

$$X^{P2}i = X^S\pi(i), i = 0, 1, \ldots, K-1 \quad (1)$$

Where the relationship between the output indexes *i* and the input π (i), index satisfies the following quadratic form:

$$\pi(i) = (f1\, i + f2\, i^2) \bmod K \quad (2)$$

The parameters f1 and f2 are predefined values depending on the block size K [10].

B.Turbo Decoder

On the other side, a turbo decoder consists of two constituent decoders named as Soft Input Soft Output (SISO) decoders or maximum a posteriori (MAP) decoders [1] coupled in an iterative loop via Interleaver (π) and De-interleaver (π^{-1}) as shown in R.H.S part of Fig.2. Turbo decoding is usually followed with the algorithm proposed in [2], referred as BCJR algorithm also known as Maximum a posteriori(MAP) algorithm.

The principle of Turbo Decoding: The theme of turbo decoding, represents iteratively exchanging the extrinsic log likelihood ratios (LLRs) between the SISO decoders (SD) to improve the error rate performance successively. The LLRs implies the probability of a received bit being a binary 1 or 0. The computation operation performed by one SD is half iteration and by both SDs is referred to as a full iteration.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 3, March 2017

III. TURBO DECODER DESIGN PERSPECTIVE

A.Algorithm aspects-map

There are two prime methods for iteratively decoding recursive systematic convolutional codes, namely soft output viterbi algorithm (sova) [3] and maximum a posteriori (map) algorithm [4]. Here, sova can be implemented with a lower hardware resource and lower computational complexity but with degraded decoding performance. Map algorithm [5], a classic algorithm, traverses a trellis of transmitted code to compute forward state metrics and backward state metrics to calculate llrs and gives the best decoding performance, but it suffers from high computation complexity, latency and leads to a large dynamic range for its variables. To reduce large memory requirements and latency, two types of window based techniques namely sliding window (sw) and parallel window (pw) were widely adopted while implementing map algorithm. The sw technique is widely used to reduce the size of internal buffers, in the design of turbo decoder. The pw technique is more suitable than sw technique for the highly parallel siso architectures. Conventional map algorithm involves in complex mathematical operations such as multiplication, division and exponential [4].
Hence, for real-time implementation, new sub-optimal map algorithms have been proposed by taking map algorithm as a reference, which is logarithmic map (log-map) [26], the log-map algorithm restores multiplications with additions, and replaces additions by the max* operation to reduce computational complexity. Logarithmic transformation of this algorithm overcome such complex operations and simplifies the computation of state metric in each of the trellis states by using branch metrics and state metrics of previous state [11, 12]. But log-map algorithm approximation has high cpu running time than max-log-map algorithm. Maximum log-map (max-log-map) approximates max*(a, b) using max(a, b) to further reduce complexity but its error correction performance is lower than log-map algorithm.

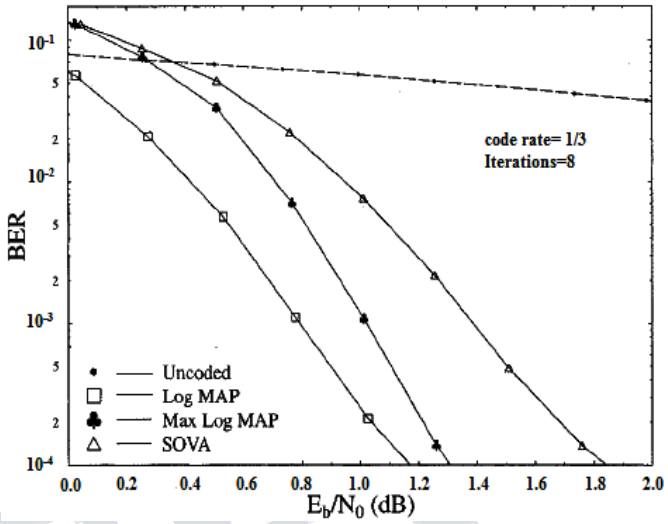

Fig. 3 ber performance of map algorithms

Max-log-map log-likelihood ratios (llrs) was derived as

$$\text{llr}(u_k) = \max_{\substack{(s',s)\\ d_k=+1}}(\alpha_{k-1}(s') + \gamma_k(s', s) + \beta_k(s)) - \max_{\substack{(s',s)\\ d_k=-1}}(\alpha_{k-1}(s') + \gamma_k(s', s) + \beta_k(s)) \quad \text{|\_\_\_\_\_(3)}$$

Where the branch metrics $\gamma_k(s',s)$ is the logarithm of transition probability from states s' to s and is obtained from the a posteriori probability and conditional probability.

$$\gamma_k(s',s) = \ln (p(y_k \mid x_k)\, p(u_k)) \quad \text{----------(4)}$$

The backward and forward state metrics in s state are

$$\alpha_k(s) = \max [\gamma_k(s',s) + \alpha_{k-1}(s')] \quad \text{----------(5)}$$

$$\beta_{k-1}(s) = \max [\beta_k(s) + \gamma_k(s',s)] \quad \text{----------(6)}$$

Two more algorithms, constant log-map (cons log-map) [27] and linear log map (lin-log-map) [28] were proposed. Bit error rate (ber) performance of map algorithms is shown in fig.3.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 3, March 2017

B.Design aspects- varios map algorithms

An effective way to realize high throughput turbo decoders is to employ multiple siso decoders in a parallel manner and those share the same input and intermediate memory [17]. But with increasing degree of parallelism, the internal latency of the siso decoders becomes a large fraction of each half- iteration. Due to iterative nature of turbo decoding algorithm, the large latency strongly affects the throughput for high code rates, which makes the implementation of high throughput turbo decoders as challenging task for high code rates. A comparable analysis of existing architectures distinctly shows that parallelism in siso decoders increases latency and hardware complexity. So, it's a challenging task to design an efficient turbo decoder design of higher data rates.

The design engineer of a turbo decoder has to consider the trade-off existence in the categories of architectural and algorithmic levels [29], as shown in the Fig. 4. Various recent VLSI implementations have been proposed by researchers to obtain high throughput with maximum possible low latency by algorithmic and architectural improvements for high-performance LTE and LTE-A Standard wireless communications. The latency of window based SISO decoder causes decreasing the throughput gains with expanding the degree of parallelism, as the system latency is directly proportional to sliding window size. There are trade-offs among a number of iterations, throughput and size of the sliding window for designing a suitable turbo decoder architecture for the physical layer.

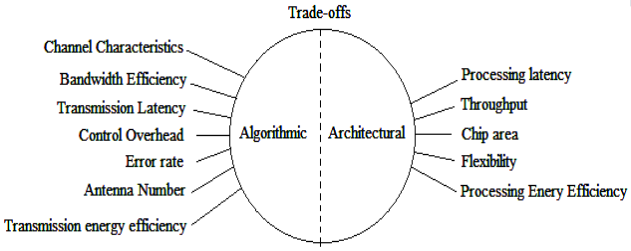

Fig. 4 Design trade-offs in a communication system.

Throughput (Θ_T) of the decoder depends on CMOS technology used, clock frequency (F) and a number of decoding iterations (ρ).

$$\Theta_T \alpha F \quad \text{and} \quad \Theta_T \alpha 1/\rho \quad \text{--------- (7)}$$

- Number of iterations of decoding cannot be altered, as it degrades the error rate performance.
- Possibility of improving throughput is by improving operating clock frequency.
- Also, by scaling down the CMOS technology, large design issue can be resolved to some extent.

Low power techniques can be incorporated into the architecture of turbo decoder while designing for performance improvement.

Even though the parallel decoders achieve higher data rates, it necessitates huge hardware resources; hence the challenging task of the turbo decoder is to design scaled-down the hardware complexity. This type of work carried out by reducing the memory need for storing the forward state metrics and branch metrics in each SISO decoder, low power track back of MAP based duo binary turbo decoders and memory reduction based on metric compression using non-uniform quantization and Walsh-Hadamard transform methods in 2011 by M. Martina [13, 14].

IV. VLSI ARCHITECTURES OF TURBO DECODER

In this regard, this section summarizes various benchmark VLSI designs of parallel turbo decoders of 4G LTE, LTE-A standard and comparative analyses of benchmark architectures are presented.

Belfanti et.al [2013] proposed a highly parallel turbo decoder 65nm ASIC design employed 16 windowed Radix-4 SISO decoders, supports 1.013 Gbps in 5.5 iterations. This design consists of 4 input RAMs, 2 intermediate RAMs, a CRC computation unit and address generators along with 16 SISO decoders, as shown in the Fig.5.

1) This design introduced optimized state-metric initialization scheme to reduce latency in SISO decoders. This scheme processes consecutive half-iterations in an *overlapping* manner, such that make use of all computational stages in SD. This method of computation eliminates SD latency on iterative decoding process and results in significant throughput gain and avoids additional silicon without any noteworthy loss in BER performance.

2) A novel CRC based early termination implementation averts decoder from redundant iterations by recognizing correctly decoded code block by applying two step CRC checksum [19].

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International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
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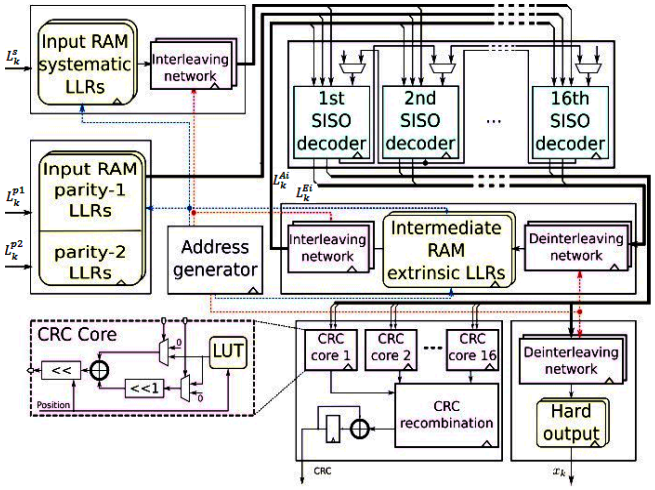

Fig. 5 Architectural diagram of Turbo decoder

G. Wang et al. [2014] proposed a flexible and efficient VLSI architecture with a 45nm CMOS technology [21]. This supports multi-standards 3G and 4G like HSPA+/LTE/LTE-A. This design has 16 radix-4 SISO MAP decoders. This work aims, to avoid severe memory conflicts problem raised by concurrent memory reading/writing in parallel turbo decoders, which is one of the major bottlenecks in high throughput decoders. Memory conflicts take place due to the randomness of interleaver /de-interleaver. Here, two individual scheduling schemes are proposed to eliminate memory reading/writing conflicts. A balanced scheduling scheme to avoid memory reading contentions and a double buffer contention free (CDBF) buffer architecture to avoid memory writing conflicts.

A balanced scheduling scheme[21] proposed here is to provide continuous read operation in next half iteration by writing the output data in interleaved/de-interleaved order in both iterations as shown in Fig.6(b). So, all the memory reading operations are continued unlike unbalanced scheduling, where both read-write operations sharing the same data from/to the memory in first half iteration then SISO decoder first reads data from memory in an interleaved way then once the computation is done, the SISO decoder writes the data to memory in a de-interleaved way; which results in memory conflicts.

A double buffer contention free buffer architecture[9] to solve memory writing conflicts .This architecture consists of FIFO and Circular built around the interleaver as shown in the Fig.7. Circular buffers built by registers to store the concurrent data write operations. All incoming data rejected LLR datum are pushed into a FIFO, to avoid overflow and writing conflicts.

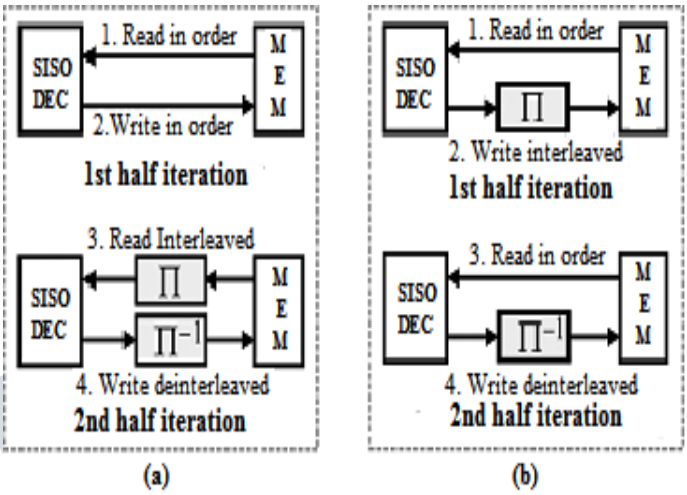

Fig. 6(a) Unbalanced scheduling 6(b) Balanced scheduling

Carlo Condo et al.[2013] particularly proposed the design of a reconfigurable architecture for both turbo and LDPC codes decoding. The novelty of this contribution is;
Firstly, introducing a formal and systematic treatment to tackle the reconfiguration issue and secondly, proposing flexible reconfigurable NoC-based turbo/LDPC decoder architecture with a small complexity overhead [18].

Rahul Shresta and Roy P.Paily [2014] proposed a high throughput turbo decoder with 8 and 64 parallel radix-2 Map decoder architecture in 90 nm CMOS technology [25].

This work focused on VLSI design for high-speed Map probability decoders using the Log-MAP algorithm. This work proposed two schemes, a new ungrouped backward recursion scheme in sliding window Log BCJR algorithm to compute backward state metrics. Secondly, a new state metric normalization technique applied in Add Compare Select Unit to reduce the critical path delay. These two techniques offer retiming and pipelining in architecture for performance improvement. Thirdly, this work adopted fine grain clock gating technique to solve power issue.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 3, March 2017

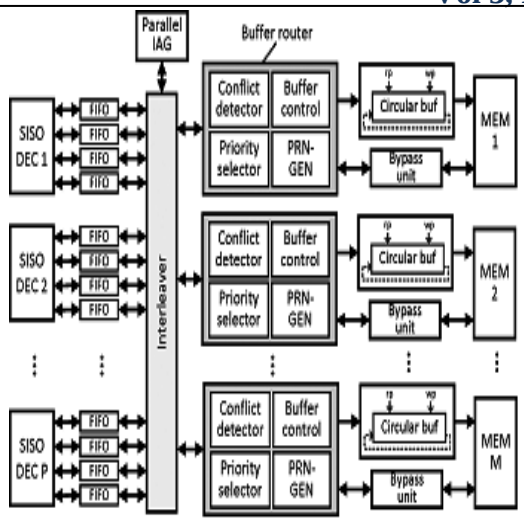

Fig. 7 DBCF architecture

Jing-shuin Lin et al.[2015] proposed a highly parallel turbo decoder structure to achieve highest throughput rate of 1.45Gbps implemented in 90 nm CMOS technology. This work aims to improve the decoding efficiency and this improvement is possible by modifying the parallel window MAP decoding algorithm. In this work, a dummy calculation reduced parallel window (DCR-PW) MAP decoding algorithm is proposed, which reduces the dummy recursion adopted to make sure the convergence of backward/forward metrics. This technique is useful in highly parallel decoders than sliding window based turbo decoding. Also, this work uses a reasonable size of metric memory and an appropriate parallelism P to support various rates and block lengths [22]. The decoder architecture consists of a Turbo controller, a switch circuit, a QPP interleaver address generator, a larger size extrinsic memory and P parallel SISO decoders, as shown in Fig. 8. Here turbo controller sends decoding signal to start decoding process in conformity with the assigned data, then a priori information for the next iteration. This process continuous till the maximum iteration is reached.

An Li et. All [2016] proposed a fully parallel turbo decoding algorithm [24], which allows parallel processing to offer higher processing throughput, unlike conventional MAP decoding algorithm which owning to the serial data dependencies. This novel FPTD algorithm reduces 50% of computational complexity and enhances its suitability for FPGA implementations. The FPTD algorithm adopts the concept of equivalent logic blocks, this logic block corresponds to a pair of 4 input Look Up Tables (LUTs) and a register or 6 input Look Up Tales and a register. Pipelining of the loading, processing and pushing out the

outputs is allowed when decoding several successive frames.

Benkeser et. Al. [2009] had proposed radix-2 non-Parallel turbo decoder architecture, using a max-log-Map algorithm. It achieved a throughput of 20.2 Mbps, suitable for HSDPA wireless communication standard and it occupies less silicon area [15].

In 2009 Ref [17], Kim et al. proposed a radix-4 architecture of turbo decoder with 8 SISO decoders in parallel to achieve 100 Mbps throughput using the Max-log-Map algorithm. This realization of SISO parallel structure occupies design area 10.7mm^2 [2009].

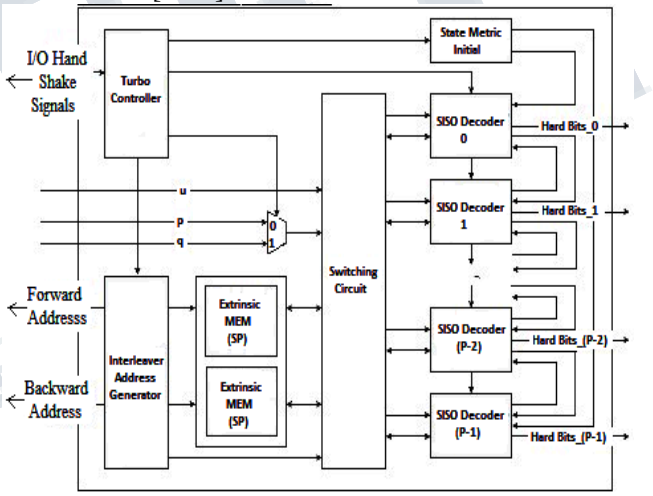

Fig. 8 Proposed architecture of Turbo decoder [22].

Ref [18], Studer et al. designed a radix-4 parallel turbo decoder architecture using the Max-log-Map algorithm to achieve a throughput of 390 Mbps, implemented in 130 nm CMOS technology, where the pipelining concept is applied to master-slave batcher network to have parallel and interleaved access to memories at high throughput [2011].
Table-1 compares various design characteristics of State-of-the-art LTE standard turbo decoders based on various MAP algorithms.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 3, March 2017

Table IComparison of Benchmark FPGA implementations of Turbo decoders

Implementations	Comparison for LTE Code standard Turbo Decoder							
	An Li 2016[23]	*An Li 2016[24]*	*Jing-Shi un Lin 2015[22]*	*Rahul Shreshta 2014[25]*	*Rahul Shreshta 2014[25]*	*G. Wang 2014[21]*	*S. Belfanti 2013[19] & Roth C. et al. 2014[20]*	*C. Condo 2013[18]*
Algorithm	FPTD	FPTD	Max-Log	Log-Map	Log-Map	Radix-4 XMAP	Max-Log	Max-Log
Radix/Parallelism	2/6144	2/6144	2/96	2/ 8	2/64	4/64	4/16	2/35 PEs
Technology[nm]	65	40	90	90	90	45	65	90
Clock Frequency[MHz]	100	65	250	625	625	600	410	200
Core Area[mm^2]	109	55	-	6.1	19.75	2.43	2.49	4.87
Power[mW]	9618	-	-	272.04	1450.5	870	966	183.2
Throughput[Mb/s]	1580	1530	1455	301.69	2274	1670	1013	292
Voltage[V]	1.08		-	1.0	1.0	0.81	1.2	-
Iterations	39	28	5.5	8	8	5.5	5.5	8
Gate count	-	-	6677k	694k	5304k	1470k	1574k	-
Sliding window size	-		32	32	96	-	14-30	-
Normalized area[mm^2/Gbps]	6.9	-	-	--	-	1.46	2.46	3.6

V. CONCLUSION

In the present wireless communications, high throughput design and implementation have become a dominating necessity in the field of VLSI design for advancing wireless communication systems. There has been a high-speed flow in data-rate for next generation wireless communications and this will open on to more complex algorithms and VLSI architectures in next few decades. Based on this framework, the present study on turbo code and the various design aspects of high throughput turbo decoder have been furnished. So that, it is indispensable to inspect both algorithmic design and architectural sides to achieve the best design that reaches the demands of succeeding generation technology.

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