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A High Gain Low Power CMOS Operational Amplifier

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Abstract: **-- This paper presents the design and simulation of a high gain low power complementary metal oxide semiconductor operational amplifier in 90nm technology. The aspect ratios of all the transistors were designed. High gain allows the operational amplifier (op-amp) circuit to function efficiently in a closed loop feedback system, whereas wide bandwidth makes the circuit to operate for high speed applications. The proposed op-amp design consists of two stages and operates at 1.2V power supply. It is aimed to meet a set of standard specifications. The entire op-amp design is evaluated using Cadence software tools, while the layout has been developed using Virtuoso. The op-amp circuit is able to achieve 38 dB gain, a 4V output swing, a 12.7 V/µsecond slew rate and a CMRR of 61 dB with a power supply voltage of 1.2 V.**

Keywords**- Slew rate, low power, sampling, high speed, closed loop system, bandwidth and aspect ratio.**

I. INTRODUCTION

Operational Amplifiers (Op-Amps) circuits are one of the important and basic components in various mixed signal systems. They are used in in many applications such as in voltage reference circuits, analog-to-digital converters (ADCs), digital to analog converters (DAC), Phase locked loops, realizing different filter circuits, voltage controlled oscillators, and switched capacitor circuits etc. General purpose op amps can be used as buffers, summers, integrators, differentiators, clippers, clampers, comparators, negative impedance converters, and many other applications. Using only a few resistors and capacitors connected externally to the op-amp, it can serve vital tasks such as amplification, filtering and phase shifting of the signals etc. Today op-amps are widely used in all wireless communication devices. Initial op-amps were designed and implemented using bipolar junction transistors. Later complementary metal-oxide semiconductors (CMOS) technologies evolved and became popular as lower-power digital-logic alternatives to transistor-transistor logic (TTL). Contrast to other transistor types, CMOS transistors only draw current when switching states, hence, they consume low power. With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, miniaturization in transistor scaling, and the developments in fabrication processes, the integrated circuit market is growing rapidly. The International Technology Roadmap for Semiconductors (ITRS) indicates that the supply voltage will be scaled down to less than 1V for high-performance/low power analog circuit designs by the year 2019. Although the reduction in supply voltage (VDD) is beneficial for digital design, whereas in analog circuit design it becomes increasingly difficult to achieve the optimum performance. This is because most of the circuit techniques that are being used today may become unusable in the circuit designs targeting deep sub-micron processes. So there is need to develop new circuit techniques, process parameters and architectures.

With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to design. Scaling down of CMOS feature sizes results in higher unity gain frequency (fT) which means the transistors operate faster than before. However, this is achieved at the cost of a reduction in transistor's open loop gain (AOL). Also due to scaling power supply voltage can be reduced. So because of this the weight and size of the battery reduces and enables longer battery life time. Hence for the same reason, low-powered circuits reduce thermal dissipation. Thus amplifiers designed in smaller device lengths exhibit larger bandwidths but lower open loop gain [1-2]. Finally in most of the mixed signal systems, the overall system performance is strongly influenced by the performance of the Op-Amp

This paper is organized as follows. Section II discusses the previous works related to the design of two stage op-amp. Section III presents theory related to CMOS op-Amp. Various parameters of op-amp have simulated and presented in section IV. Finally, conclusions are drawn in Section V.

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II. RELATED WORKS

V. Ivanov et al [1] presents an ultra-low power reverse bandgap voltage reference operational amplifier operated from supply voltages of the order of 0.75V. This proposed reference circuit is a part of microprocessor system on chip implemented in a digital 130 nm CMOS process and occupies a total area of 0.07 mm2. The obtained reference accuracy is ± 2.5% over a temperature range of (-20°C to +85°C) without trimming. With trimming ± 0.5% accuracy is achieved. George Raikos et al [2] propose a low-voltage bulk-driven CMOS operational amplifier. The inherent small signal transconductance of the bulk-driven devices is enlarged using a positive feedback, and also the noise performance is improved. The amplifier is designed using standard 180nm n-well CMOS process. The amplifier is optimized to operate at 0.8 V supply voltage, and it is also capable to operate at power supply voltage of 0.7 V. The proposed amplifier consumes an operating current of 130 µA, has a open-loop gain of 56dB, 154 nV/√Hz input-referred spot noise at 100 kHz, 80 dB CMRR at 100 kHz and IIP3 equal to −4.7 dBV. J. M. Carrillo et al [3] presents a CMOS operational amplifier with rail-to-rail input and output voltage ranges, suitable for operation in extremely low-voltage environments. The method is based on a bulk-driven input stage with extended input common-mode voltage range, in which the effective input transconductance is enhanced by means of a partial positive feedback loop. Due to this the performances of gain and gain-bandwidth product are similar. Output rail-to-rail operation is achieved by means of a push-pull stage, which is biased in class-AB by using a static feedback loop, thus avoiding frequency limitations inherent in dynamic-feedback tuning schemes. The proposed two-stage operational amplifier was operated from 1V power supply, and a test chip prototype was fabricated in 350nm standard CMOS technology. The experimental performance features an open-loop DC gain higher than 76 dB and a closed-loop unity-gain bandwidth above 8 MHz when a 1-MOhm, 17-pF load is connected to the amplifier output. T. Stockstad et al [4] describes a 0.9V 0.5µA, rail-to-rail CMOS operational amplifier based on weak inversion techniques. Depletion-mode nMOS transistors buffer a bulk-driven pMOS differential pair to realize wide input dynamic range, while the output stage architecture provides symmetric rail-to-rail output drive through the use of a low-voltage translinear control circuit. Fırat Kacar et al [5] propose a new biquad filter configuration using a Voltage Differencing Buffered Amplifier (VDBA). This proposed block has high impedance at its input terminals and low impedance at output terminal. Besides, VDBA has a transconductance gain, thus the proposed circuits can be employed without using any external resistors. Also in this paper, two new voltage-mode biquad filter configurations are presented for VDBA application. Each proposed filter employs two active elements and two or three passive components. Filters, having three inputs and single output, can realize voltage mode low-pass, band-pass, high-pass, band-stop, and allpass filters. For the second biquad, quality factor can be adjusted via resistor independently of the natural frequency. Simulation results are given too, confirming the theoretical analysis. The proposed biquad filters are simulated using TSMC CMOS 360nm technology.

III. CMOS OPERATIONAL AMPLIFIER

An ideal operational amplifier has infinite voltage gain over an infinite bandwidth, infinite input resistance, infinite slew rate, infinite common mode rejection ratio, zero offset voltages, zero offset currents and zero output resistance [7]. The functional block diagram of general two stage operational amplifier is shown in figure 1. The first stage is a differential input stage which provides the required high gain for the op amp and can also performs the differential-input to single-ended output conversion. This stage has the most dominant pole of the system. The second stage is usually an inverting stage and can offer high gain as well as differential-to-single ended conversion if necessary. Op amps that need to drive small resistive loads also include a buffer/output stage that drives the load and determines the output swing. The third stage is most a unity gain source follower with a high frequency and negligible pole. The compensation circuitry usually consists of a capacitor that ensures frequency stability when the op amp is used in a negative feedback network. Joining the input and output nodes of the second stage results in a phenomenon known as pole splitting. This phenomenon lowers the pole or bandwidth of the first stage and moves the pole of the second stage to a higher frequency which helps the op amp to achieve required stability in the presence of negative feedback. Pole splitting technique is a useful technique in designing amplifiers at higher frequencies, but requires a capacitance and a resistance for proper compensation of MOSFET op amps

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and, thus, the whole circuit becomes complex. The main limitation is the value of compensating capacitor, as it is directly related to the size of the chip area.

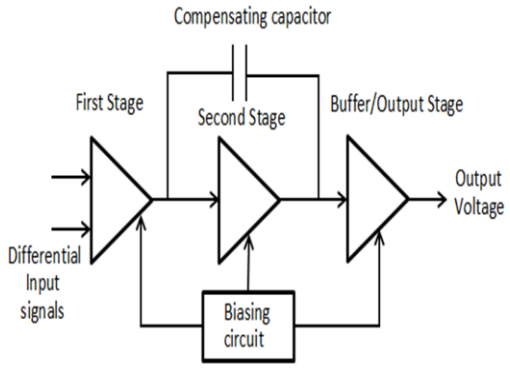

Figure 1: Block diagram of Operational Amplifier

The purpose of biasing circuitry is to provide a stable, quiescent operating point for the entire circuit. The dynamic range of an op amp is controlled by the op amp's offset voltage, noise, input common-mode range (ICMR) and output swing. The ability of the op amp to provide an accurate closed-loop gain is dictated by the open-loop gain (AOL). The frequency response of the circuit is characterized by the small-signal bandwidth, phase margin, settling time and also large signal bandwidth. The range of maximum and minimum voltages that can be obtained without any clipping at the output is characterized as output swing. Slew Rate is the maximum rate of change of output voltage with respect to time. The ability of an op amp to prevent its output from being affected by any variation in the power supply voltage is characterized as power supply rejection ratio (PSRR). Figure 2, shows the circuit diagram of CMOS operational amplifier [6].

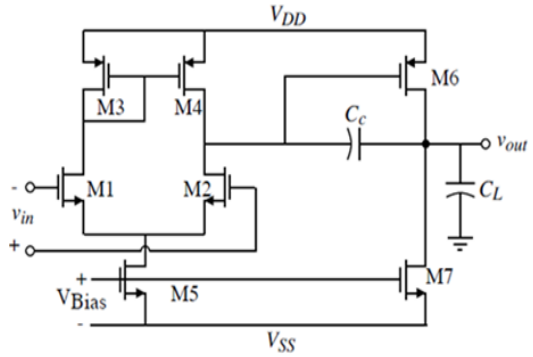

Figure 2: Circuit diagram of CMOS Operational Amplifier

IV. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

The circuit schematic of CMOS operational amplifier shown in figure 3 is simulated using Cadence spectre schematic editor, while the layout has been developed using Virtuoso. The simulated response for Transient analysis, AC analysis (Magnitude and Phase response), Noise analysis and Fourier analysis are shown in figures 4, 5, 6 and 7.

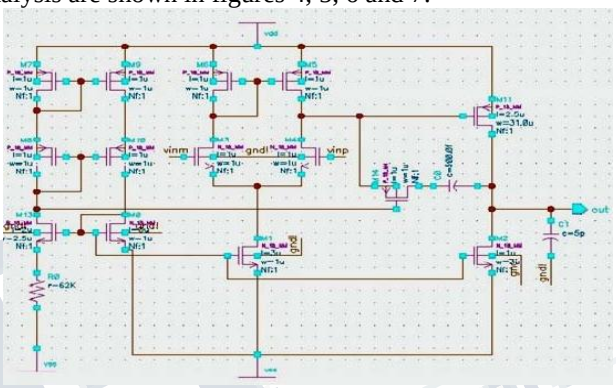

Figure 3: Schematic diagram of Operational Amplifier

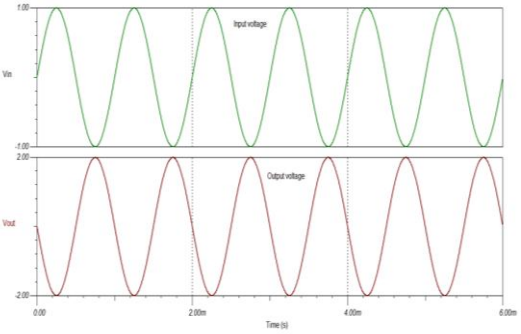

Figure 4: Transient Analysis

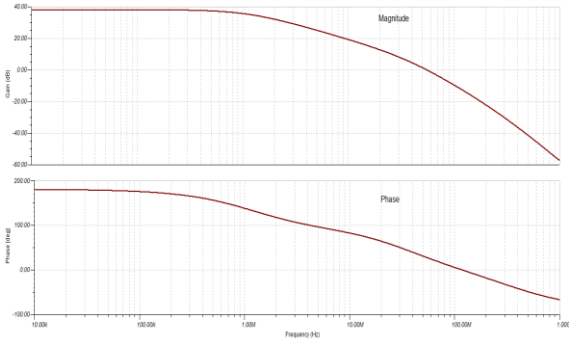

Figure 5: Magnitude and Phase response

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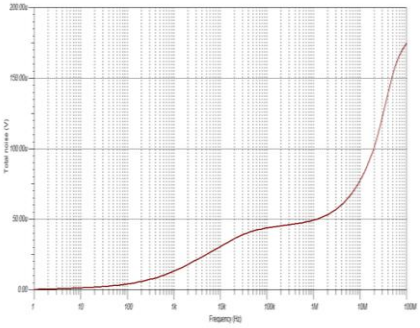

Figure 6: Noise Analysis

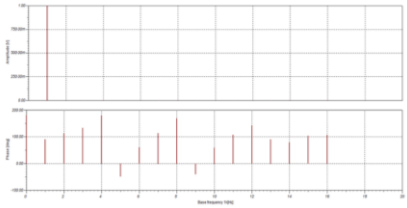

Figure 7: Fourier Analysis

The simulated parameters of the CMOS operational amplifier are shown in Table 1.

Table 1: Simulated Op-Amp parameters

Parameter	Simulated results
Technology	90nm CMOS
Operating Supply Voltage	1.2V
Gain	38dB
Slew rate	12.7 V/µsecond
Unity Gain bandwidth	55MHz
CMRR	61dB
Phase Margin	43 degree
Input swing	+/-1mV
Output swing	+/- 2V
Power dissipation	1.1µW
Area	10µm × 9µm

The layout of the operational amplifier is shown in figure 8.

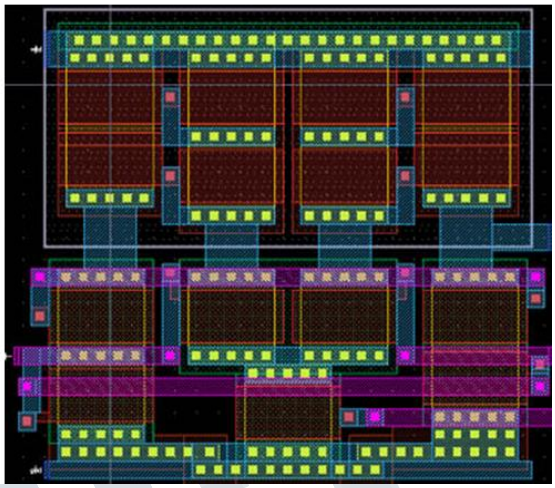

Figure 8: Layout of the designed Operational Amplifier

V. CONCLUSIONS

A high speed low power two stage operational amplifier in 90nm CMOS technology is designed and simulated results are shown in this paper. From the simulation results it is observed that the designed op-amp attains high gain, low power and occupies less area. Hence it can be used for high speed wireless portable applications. In this paper a miller compensation technique has been employed to improve the stability of the system. The circuit can be redesigned to operate at higher speed by changing the aspect ratios of the transistors. The gain of the op-amp can be increased further by cascading another device in the input stage. Also the output voltage swing may be increased by using a double ended output.

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