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Design and Implementation of Serial Protocol Convertor/Translator on FPGA

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Abstract: **- In the world of multiple application based product it is very much a mandatory to have multiple devices connected to a system, this includes peripherals following different communication protocols as well. These requirements give rise to the need for an intermediate system which can act as a bridge between two devices following different communication protocols. Today a system is connected to a number of devices and makes the communication smooth and fast. Communication protocols such as I2C, SPI and UART protocols are commonly used protocols. The PC, ADC and DAC will require an interface for communication between them. It is used to minimize system-level interconnect. FPGA is mainly uses serial communication to communicate with peripherals. Therefore serial communication plays vital role in embedded system design. In this paper we focus on the implementation of protocol converter to convert standard protocol of one device to the protocol of other device [SPI, UART, and I2C].The proposed work simulated by using VHDL code in Xilinx 14.7i and implemented on Spartan 3E FPGA.**

Keywords: **-- Protocols, Bluetooth module, FPGA Kit, Android mobile phone.**

I. INTRODUCTION

FPGA is mainly uses serial communication to communicate with peripherals. Therefore serial communication plays vital role in embedded system design. In this paper we focus on the implementation of protocol converter to convert standard protocol of one device to the protocol of other device [SPI, UART, and I2C].The proposed work simulated by using VHDL code in Xilinx 14.7i and implemented on Spartan 3E FPGA.A system is connected to a number of devices and makes the communication smooth and fast. Communication protocols such as I2C, SPI and UART protocols are commonly used protocols. The PC, ADC and DAC will require an interface for communication between them. It is used to minimize system-level interconnect. FPGA is mainly uses serial communication to communicate with peripherals [1]. The rest of paper is structured as follows. Section 2 gives summary of protocols and others, and Section 3 presents the types of protocols. Section 4 describes Existing system of protocol convertor on FPGA and also some limitations of this system, Section 5 describe the proposed system of protocol convertor/translator and mainly some advantages, applications. Section 6 gives simulation results and Section 7 provides conclusion of the paper.

II. RELATED WORK:

The oscilloscope is the basic instrument for the study of all types of waveforms. It is capable of generating a graph of an input signal versus time (Voltage-time mode), or a second variable (X-Y mode). It can be employed to measure such quantities as peak voltage, frequency or period, phase difference, pulse width, delay time, rise time and fall time. While SPI, as well as others serial protocols such as I2C and 1-wire for instance, are well suited for communications between integrated circuits for low/medium data transfer speed with on-board peripherals. Consequently, when there is a need to implement a communication between an integrated circuit such as a microcontroller and a set of relatively slow peripherals, there is no point in employing any excessively complex protocols. In this case, SPI stands among the best candidates. This is why it becomes a worldwide standard for modern digital electronics systems and it will probably continue to compete in the future The design of i2c master controller has immense applications in future as the number of devices connected to a system is only going to increase. This is just two wires, called SCL and SDA. SCL is the clock line. It is used to synchronize all data transfers over the I2C bus. SDA is the data line. The SCL & SDA lines are connected to all devices on the I2C bus. There needs to be a third wire which is just the ground or 0 volts. There may also be a 5volt wire is power is being distributed to the devices. Both SCL and SDA lines are "open drain" drivers.

III. TYPES OF PROTOCOLS:

This paper consists more protocols to transfer the data one chip to another chip. These protocols are SPI

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Protocol, I2C Protocol and UART Protocol; it describes more accuracy and speed.In the world of multiple application based product it is very much a mandatory to have multiple devices connected to a system, this includes peripherals following different communication protocols as well. This requirement gives rise to the need for an intermediate system which can act as a bridge between 2 devices following different communication protocols. This is where I2C master controller design is very useful. Today a system is connected to a number of devices and makes the communication smooth and fast, I2C protocol is considered as one of the very best. But there are number of devices which follow SPI protocol as well. So such devices can be considered as a slave. The I2C master controller on one end is connected to a PC or microprocessor, and on the other end it will be connected to the SPI slave. Its main function will be, to understand the control register transmitted by PC and convert it into SPI control signals.

The PC connected to the controller sends data serially and every 8 bits corresponds a value specified by the i2c protocol. The address and the chip select signal select the I2C device. In this design both chip select and address of the device are default to 1, as the design is for a specific slave only. Every set of 8 bits which corresponds to a control registers which controls the flow of data, is stored in registers. A counter is initialized after successful transmission of 8 bits from the PC to the controller. As the complete set of control registers are transmitted, all the values of the registers are inverted and stored in a 32 bit register. 32 bit registers are decided on the basis of SPI slave as there are only 4 control register before the data register. Every bit of the 32 bit register corresponds to a specific signal of SPI protocol. Once the 32 bit register is fed by the corresponding registers, the serial transmission takes place, which is the MOSI input of the SPI slave. A clock signal is also transmitted to the SPI slave as SCLK which acts the main clock for the slave. This is just two wires, called SCL and SDA. SCL is the clock line. It is used to synchronize all data transfers over the I2C bus. SDA is the data line. The SCL & SDA lines are connected to all devices on the I2C bus. is often considered as “little” communication protocol compared to Ethernet, USB, SATA, PCI-Express and others that present throughput in the ×100 Mb/s range, if not Gb/s. It is important to not forget the purpose of each protocol. Ethernet, USB, and SATA are meant for “outside the box communications” and data exchanges between whole systems. While SPI, as well as others serial protocols such as I2C and 1-wire for instance, are well suited for communications between integrated circuits for low/medium data transfer speed with on-board peripherals.

Consequently, when there is a need to implement a communication between an integrated circuit such as a microcontroller and a set of relatively slow peripherals, there is no point in employing any excessively complex protocols. In this case, SPI stands among the best candidates. This is why it becomes a worldwide standard for modern digital electronics systems and it will probably continue to compete in the future.The three bus lines are as follows: SCLK - the clock signal used for synchronizing data transfers. It is generated by the bus Master

MISO - Master In Slave Out. Line used for sending data from a slave to the master.

MOSI - Master out Slave In. Line used for sending data from the master to a slave.

The data is transferred through a simple shift register transfer scheme where the data is clocked into and out of devices on a first-in, first-out basis.

IV PROPOSED SYSTEM:

SPI interface which is the full-duplex and three lines synchronous serial peripheral interface was firstly presented by the Motorola. It adopts the model of master-slave architecture and supports multiple slave devices and usually only single master. The clock is controlled by a master device. Data transmits according to the bit under the clock pulse. The rate of communication is up to 10 Mbps. The SPI protocol has been widely used for its simple interface, convenience to the hardware design and implementation, high speed of clock and less system cost. But SPI has serious shortcoming.

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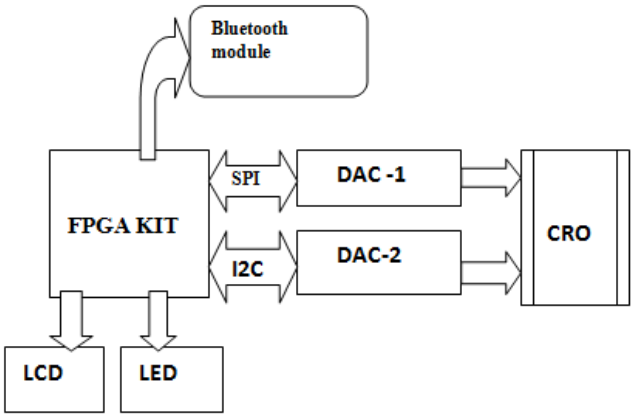

Fig. Block diagram

First of all, it has no appointed flowing control, so that there is no response to confirm whether it has received the data; Secondly, it has no the mainly device protocol, therefore the complicated software and external logic must be used to realize the main component architecture . Device Net is a high-level industrial field bus communication protocol based on CAN bus. In 1994, it was initially proposed by the United States Rockwell Automation company, managed and popularized by ODVA organization.

The design of i2c master controller has immense applications in future as the number of devices connected to a system is only going to increase. So there is always a need for a system which supports multiple protocols. In all these situations, I2C master controller acts as a great support and will be a key in future design to support parallel functions. I2C master controller is successfully designed in VHDL and simulated in ModelSIM. Simulation results verify that the communication has been established between the microprocessor and the controller. Data processed and the output has been successfully verified as per SPI slave input. The design meets timing constraints and there are no timing violations. And all these have been achieved with minimal utilization of resources.

The PC connected to the controller sends data serially and every 8 bits corresponds a value specified by the i2c protocol. The address and the chip select signal selects the I2C device. In this design both chip select and address of the device are default to 1, as the design is for a specific slave only. Every set of 8 bits which corresponds to a control registers which controls the flow of data, is stored in registers. This is just two wires, called SCL and SDA. SCL is the clock line. It is used to synchronize all data transfers over the I2C bus. SDA is the data line. The SCL & SDA lines are connected to all devices on the I2C bus. There needs to be a third wire which is just the ground or 0 volts. There may also be a 5volt wire is power is being distributed to the devices. Both SCL and SDA lines are "open drain" drivers. What this means is that the chip can drive its output low, but it cannot drive it high. For the line to be able to go high you must provide pull-up resistors to the 5v supply. There should be a resistor from the SCL line to the 5v line and another from the SDA line to the 5v line.

A system is connected to a number of devices and makes the communication smooth and fast. Communication protocols such as I2C, SPI and UART protocols are commonly used protocols. The PC, ADC and DAC will require an interface for communication between them. It is used to minimize system-level interconnect. FPGA is mainly uses serial communication to communicate with peripherals. The implementation of protocol converter to convert standard protocol of one device to the protocol of other device [SPI, UART, and I2C]. The proposed work simulated by using VHDL code in Xilinx 14.7i and implemented on Spartan 3E FPGA.

Advantages:

1. More than one protocol can be used in one system, i.e. more accuracy to the data
2. Operating frequency is 24MHZ or 50 MHZ
3. The cost of the system is low, because of many protocols can be used in one processor at serial communication
4. I2C Consists only two data lines
    a. SDA
    b. SLK
5. FPGA acts as both Master and Slave, So DAC returns the Ack to the FPGA

Applications:

1 Generally I2C is used in EEPROM applications
2 SPI can be used in SD Cards
3 Both SPI and I2C used in ADC,DAC Circuits
4 Data transferring cable.

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V. SIMULATION RESULTS:

By using STM32 MCU to design a device net SPI convertor. Generally we have more protocols, to convert the data one system to another.A system can be operated one protocol and also multi protocols used at a time by using FPGA Kits. By using different modules to convert the data from system to another system. More than one protocol can be interfacing the FPGA kits, I2C and SPI protocols are used. These protocols are used data transfers fastely, efficiently.By using Xilinx 14.7i all modules can be programming and assigned for some observations, these observations are RTL Schematic and LTI Schematic Diagrams.Finally program can be simulated and also synthesis, to observe the output waveforms.

Output Waveforms

The proposed Serial protocol convertor is better Area and Delay characteristics when compared to existing system. The complexity is also reduced when compared to the other communication protocols.

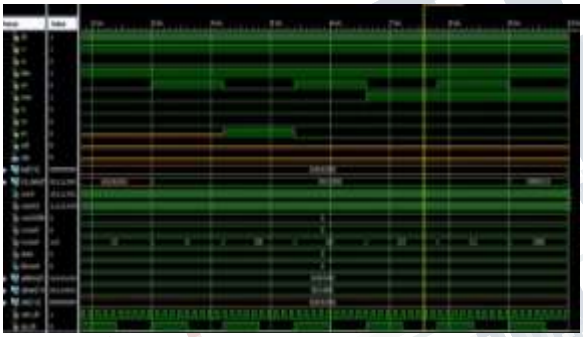

Fig. Simulation results for proposed system

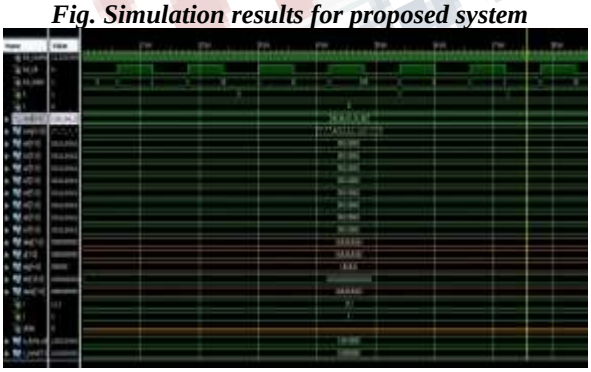

Fig. Simulation results for proposed system

Fig. Power consumption in proposed system

Simulation is the process of functional verification of the given input circuit. Design and implementation of serial protocol convertor by using single FPGA KIT, on that design more number of protocols can be used.

VI CONCLUSION

A very simple method to implement the serial protocol conversion/translation by using FPGA kit. More protocols can be used in a single FPGA kit, and at a time more information to be transferred from android mobile to kit. Same as the output can be shows in digital CRO's. By applying any value to the android mobile to Bluetooth module, in same as the ASCII value shows in LCD display. To analyzing the output value by using digital CRO's.

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