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Standard Cell Based an Area Efficient, 1 MHz to 2 GHz Range nine- input Programmable Frequency Divider for Phase Locked Loop (PLL) Applications

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***Abstract:* -- A Programmable Frequency Divider (PFD) is proposed in this paper. First the number of inputs for PFD are increased by using asynchronous counter ,reload generator and duty cycle correction circuit`s. Second the area of PFD is reduced using standard cell layout technology. This design is implemented with 0.9volts power supply,it can be operated from 1MHz to 2GHz and the division ratio ranges from 1 to 511 at 1.25 GHz of input clock and output duty cycle ranges from48.47 to 52.22, the total power consumption of proposed programmable frequency divider is only 0.176 mW at 1.25GHz and active die area 0.000048204 mm^2.**

***Index terms:* -- Duty-Cycle Improved Circuit (DCIC), Duty-Cycle Corrector (DCC).**

I. INTRODUCTION

A phase-locked loop (PLL) is an electronic circuit with a voltage-controlled oscillator (VCO) that constantly adjusts its output phase and frequency to match (and thus lock) the reference clock signal. Phase-locked loops are widely used in radio, telecommunications, wireless communications, computers, and other electronic applications. They generate stable frequencies, modulate or demodulate a signal, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors. Since one or more complete phase-locked loop circuits can be integrated into an IC, the circuit become widely used in modern electronic devices, with output frequencies from the fraction of a cycle per second up to the gigahertz range. Frequency dividers are widely used in many communication systems such as frequency synthesizer, time-recovery circuits and clock generation circuits. In a phase-locked loop (PLL), a frequency divider is to divide down the local oscillation frequency generated by the voltage-controlled oscillator (VCO) to make a comparison with the reference frequency. The programmability provided by the frequency divider leads to different locking frequencies of the PLL.

II. BASIC BUILDING BLOCKS FOR NINE INPUT PROGRAMMBLE DIVIDER

Basic building blocks which are used in this design are asynchronous counter, reload generator, programmable counter and duty-cycle correction circuit.

A. Asynchronous Counter:

The counter used in the design is nine input down counter, which consists of D flip flops with feed-back given from complemented output. Change the decimal number into n digit binary number written from right to left in increasing powers of 2. Therefore, n divide-by-two stages gives quotient(Q) either 0 or 1 forming an n-bit asynchronous counter, where the Q[1:n] is the binary counting result. Generally, the asynchronous counter counts down from 2^n - 1 and generates result Q[1:n] to control the reload generator.

B. Reload Generator:

The reload generator comprises 2n transmission gates as switches, n NMOS transistors, and aturned-on PMOS transistor as the pseudo-NMOS logic. Every two transmission gates and one NMOS transistor form a XOR gate. When the Q_n and IN_n signals differ at the signal level, the NMOS transistor turns off and the turned-on PMOS transistor charges the signal Reload to high. Thus, all the NMOS transistors of the reload generator are turned off and

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the signal Reload will reload the asynchronous counter when the asynchronous counter counts to the complement of IN[1:n].

C. Programmable Counter:

The proposed PC not only maintains the full-range division, but also adopts a low-area design and can be easily extended to higher division ranges using the simplify reload generator as shown in fig 1. Only a D flip-flop, two transmission gates, and a NMOS transistor are required to add one bit. Furthermore, because the input clock Finis connected to the D flip-flop, which is triggered by the rising edge, the output duty-cycle is not affected by the input regardless of the input duty-cycle. However, the reload signal of the proposed PC provides anarrow output duty-cycle because the output clock has a high level only when the reload generator reloads the asynchronous counter. Fortunately, this disadvantage can be avoided by using a duty-cycle corrector (DCC). In this work, a duty-cycle improved circuit (DCIC) that is based on the concept of proposed PC has been presented to improve the output duty-cycle to 50%.

D. Duty-Cycle Correction Circuit:

The duty reload generator also uses a transmission gate and NMOS transistor to form n-1 XOR gates. The output control logic comprises a D flip-flop, a switch S1, and three NMOS transistors. The key characteristic of this circuit is that the binary shifting caused by the binary code shifting slightly to the right is the same as altering the value by half. For example, assume the input divisor is 256, the binary code of 256 is (100000000)2and the half value of 256 is 128. The binary code of 128 is (010000000)2, which is the same as when a binary code of 256 shifts slightly to the right for one bit. Thus, the signal IN[2:n] of the duty reload generator is shifted right a XOR gate to alter the input divisor to half its original value, as shown in Fig. 2. However, binary shifting cannot provide accurate changes when the input divisor is an odd number. Therefore, two NMOS transistors Maand Mband a switch S1are included in the output control logic to assess the input divisor. When the PC counts to the correct results, all the NMOS transistors M_1 to $M_n$of the duty reload generator are turned off and the output control logic enters the judging mode. Because whether the input divisor is an odd or even number is decided by the least significant bit (LSB), IN1, when the signal IN1is high, the input divisor is odd, causing switch S1to to close and the NMOS transistor waiting for the input clock Finto become low. When the Finis low, the NMOS transistor Maturns off and the turned-on PMOS transistor charges the signal Duty Reload to high. When the signal IN1is low, the input divisor is even, causing switch S1to open and the NMOS transistor Mato be turned off by the NMOS transistor Mb .Then, the turned-on PMOS transistor charges the signal duty Reload to high immediately. After the assessment, the output control logic improves the output duty-cycle to 50% Using the signals Reload, Duty Reload, and a D flip-flop. When the signal Reload is high, setting D flip-flop causes the output clock $F_{out}$to charges to high; whereas when the signal Duty Reload is high, the output clock F_{out}becomes low. Meanwhile, setting $F_{out}$to high discharges the signal Duty Reload to low using the NMOS transistor Mc. This technique is similar to that of conventional DCCs, which improve the output duty-cycle using rising and falling signals. The simple topology and logic of DCIC not only corrects the duty-cycle output pulse width to approximately 50%, but also provides alow-area design that can be low area and easily extended to higher divisor ranges.

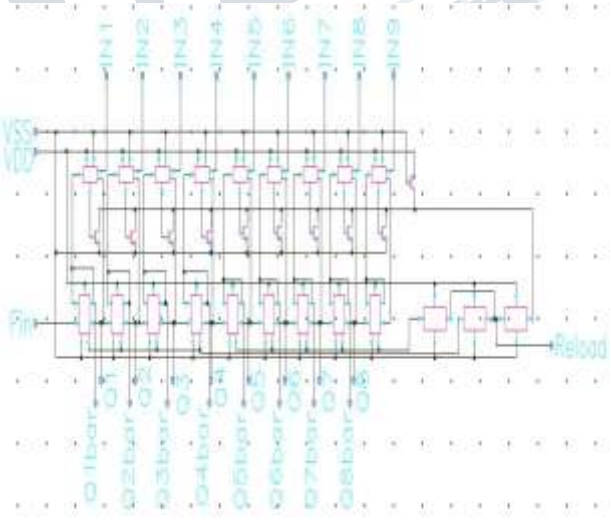

Fig. 1. Programmable counter circuit

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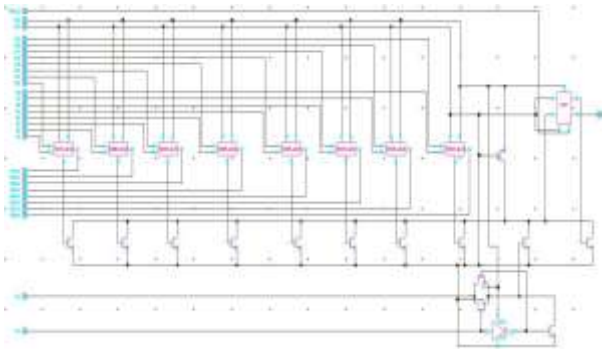

Fig. 2. Duty-cycle improvement circuit

III. PROPOSED NINE INPUT PROGRAMMABLE FREQUENCY DIVIDER

In this work, number of inputs to Programmable Frequency Divider are increased and size of this device is reduced by using standard cells.

The number of inputs are increased by using logic cells such as D flip-flop, Reload Generator, 9-Input Programmable Counter and Duty Cycle Correction Circuit. As shown fig 3The D-type flip-flop (DFF) is designed in master-slave configuration with transmission gates.The XNOR logic is implemented by using transmission gates and fig-4 shows an inverter which plays a major role in reload signal generation.XOR logic circuit is designed by using NMOS transistor to generate the reload signal which pulls the output clock to high.This reload signal strength is not sufficient to drive 9 flip-flopssimultaneously. For this reason , the buffer is used,shown in fig-6. One Buffer can drive three D flip flops. To drive nine D flip flops a total of three buffers are used.

Standard cell layout technique is used to reduce The size of the device . A standard cell is a group of transistors and interconnect structures that provides a Boolean logic function (e.g., XOR, XNOR, inverters) or a storage function (D flip-flop). The simplest cells are direct representations of the elemental XNOR, XOR and Inverter Boolean function. The cell's Boolean logic function is called its logical view: functional behavior is captured in the form of a truth table or Boolean equation (for combinational logic), or a state transition table (for sequential logic).This Standard cell is drawn for each and every component used for this device. All the standard cells are called and integrated to form the final circuit.

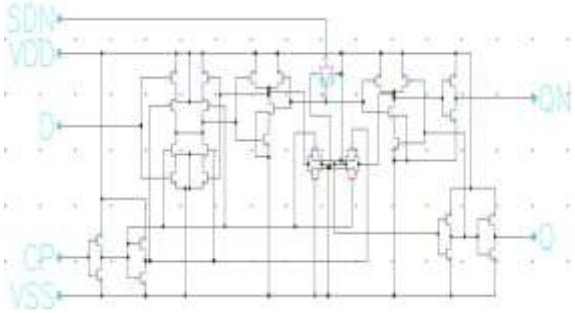

Fig. 3. Transmission gates based Master-Slave D-type Flip-Flop circuit

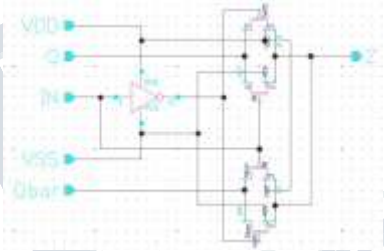

Fig. 4. Transmission gates based XNOR circuit

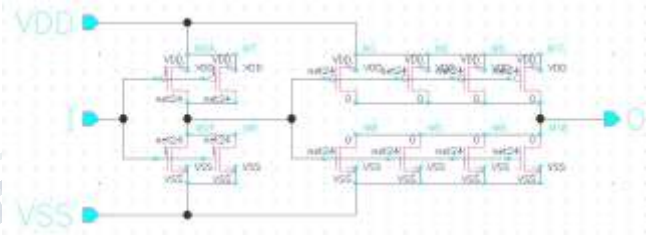

Fig. 5. Buffer circuit

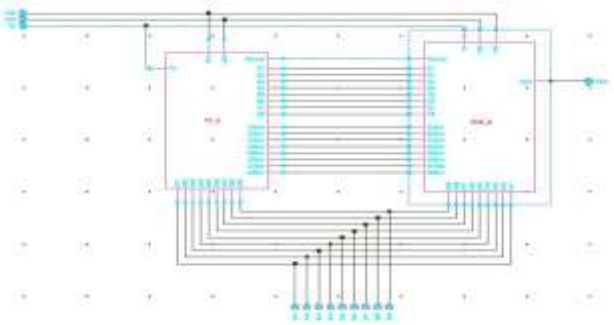

Fig. 6 The final schematic of proposed programmable frequency divider circuit

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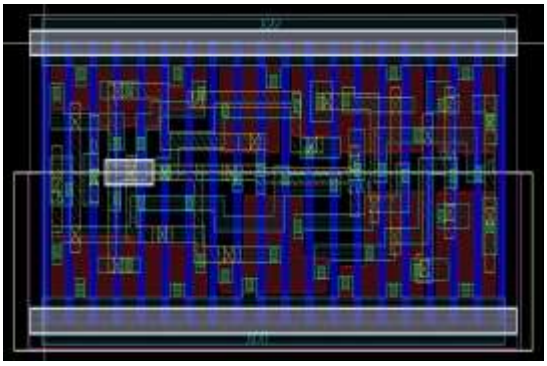

Fig. 7. Layout of D-type Flip-Flop

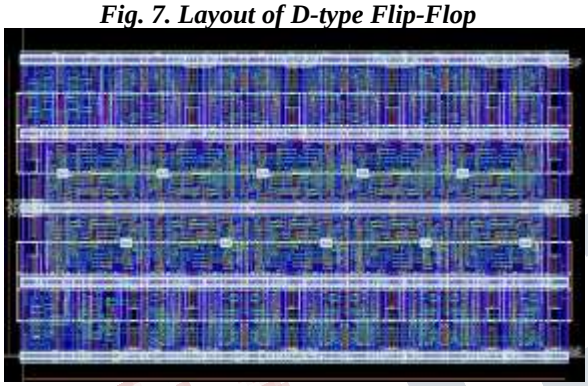

Fig.8. Layout of the proposed programmable frequency divider

IV. SIMULATION RESULTS

The proposed programmable frequency divider is implemented using a 28-nm standard CMOS technology with a supply voltage of 0.9V. The proposed programmable frequency divider layout is shown in Fig. 8.The active area is 13.39*3.6 μm^2. To compare the performance of the proposed programmable frequency divider with the previous work, a nine-stage counter is achieved in the design. Fig. 9 shows the output waveforms of the proposed programmable frequency divider when the input divisor is 511 and the F_{in} is 1.25 GHz. The output waveforms show that the output frequency of the proposed programmable frequency divider is accurate when the input frequency varies. In Addition to this, the measured mean value of the output duty-cycle at 1.25 GHz is 49.9%, achieving the desired 50% duty-cycle output.

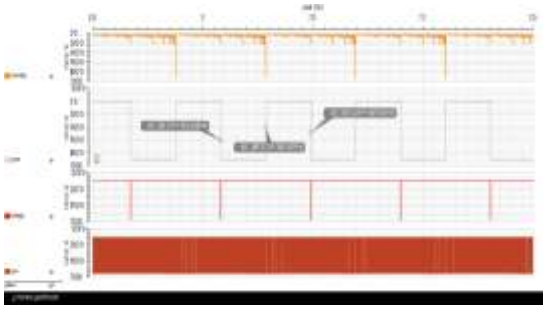

Fig.9. PFD output waveforms when the input divisor is 511 and the F_{in} is 1.25 GHz.

The output waveforms of the proposed programmable frequency divider when the input divisor is 263 are shown in Fig. 10.The F_{in} is 1.25 GHz and input duty-cycle is 25%. The output waveforms show that the proposed programmable frequency divider not only operate correctly at 1.25 GHz, and also improves the narrow duty-cycle input to 49.97% duty-cycle output.

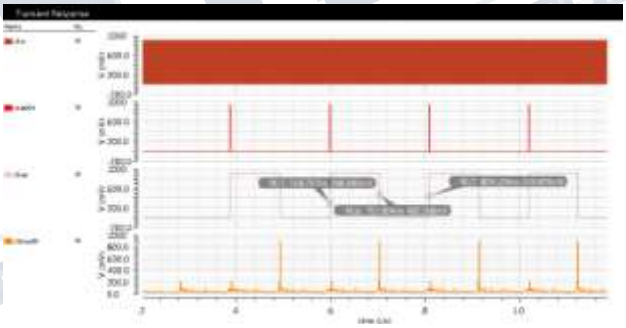

Fig.10. PFD output waveforms when the input divisor is 263 and the F_{in} is 1.25 GHz.

The output waveforms of the proposed programmable frequency divider when the input divisor is 58 are shown in Fig. 11.The F_{in} is 1 GHz, and input duty-cycle is 50%. The output waveforms show that the proposed programmable frequency divider not only operate at 1 GHz, and also improves the narrow duty-cycle input to 49.74% duty-cycle output.

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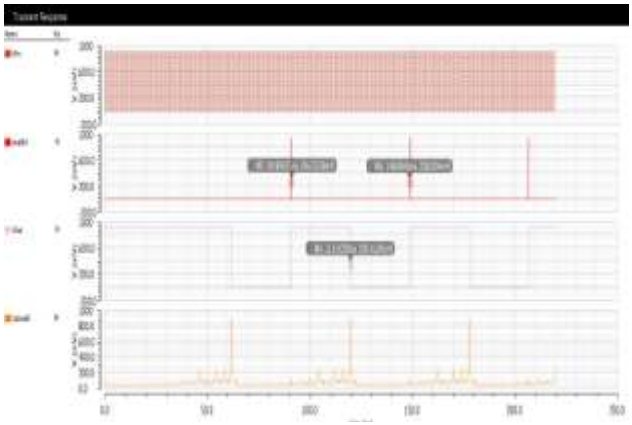

Fig.11. PFD output waveforms when the input divisor is 58 and the F_{in} is 1 GHz.

The output waveforms of the proposed programmable frequency divider when the input divisor is 126 are shown in Fig. 12.The F_{in} is 2 GHz, and input duty-cycle is 50%. The output waveforms show that the proposed programmable frequency divider not only operate correctly at 2 GHz, and also improves the narrow duty-cycle input to 50.09% duty-cycle output.

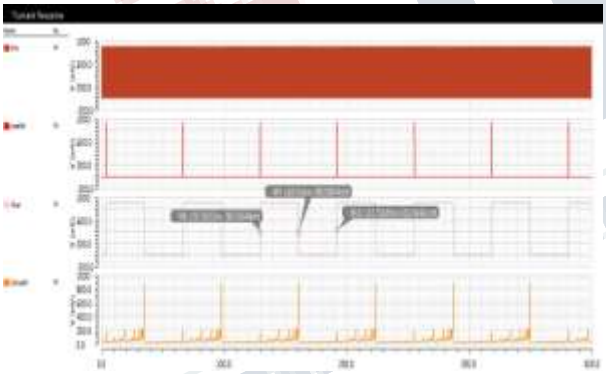

Fig. 12. PFD output waveforms when the input divisor is 126 and the F_{in} is 2 GHz.

The output waveforms of the proposed programmable frequency divider when the input divisor is 4 are shown in fig13. the F_{in} is 1.25 GHz and input duty-cycle is 50%. The output waveforms show that the proposed programmable frequency divider not only operate at 1.25 GHz, and also improves the narrow duty-cycle input to 52.22% duty-cycle output.

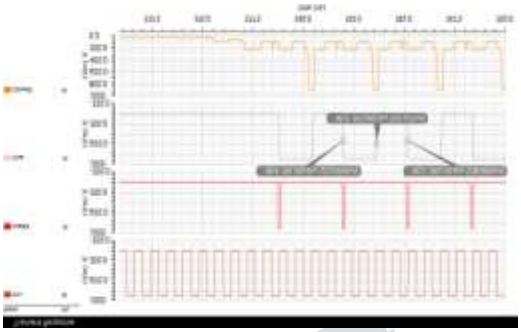

Fig.13. PFD output waveforms when the input divisor is 4 and the F_{in} is 1.25 GHz.

Fig.14 shows the output waveforms of the proposed programmable frequency divider with the input divisor 29, the F_{in} is 1.25 GHz and input duty-cycle is 50%. The output waveform show that the proposed programmable frequency divider not only operate precisely at 1.25 GHz, but also improves the narrow duty-cycle input to 49.62% duty-cycle output. The power usage of design is calculated by the tool calculator. The average of pwr signal in figure 5.21 gives the power.

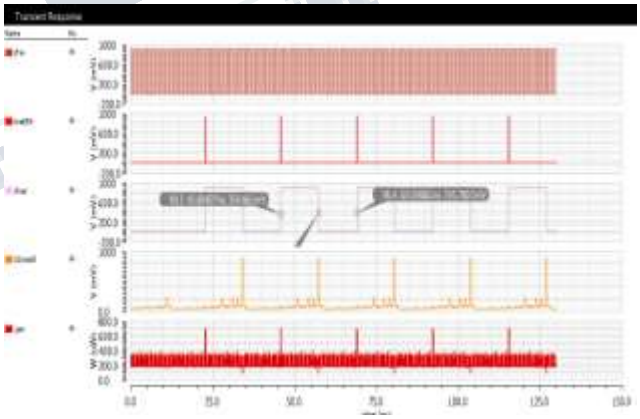

Fig.14. PFD output waveforms when the input divisor is 29 and the F_{in} is 1.25 GHz.

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Table 1 Comparison with the Results of Previous Works.

	[1]	[3]	[8]	[11]	[13]	This work
Architecture	PFD	PFD with DCC	PFD	PFD with DCC	PFD with DCC	PFD with DCC
Technology(nm)	180	180	180	180	180	28
Supply voltage	1.5	1.8	1.5	1.8	1.8	0.9
Input clock (MHz)	-3500	-2500	-3000	0.1 - 2500	1 - 1000	1 - 2000
Output Duty-Cycle(%)	N/A	44.4 - 50	N/A	33 - 66	50 - 50.7 @700MHz	48.54 - 52.22 @1.25 GHz
Core Area(mm)	0.04	0.1	0.04	0.04	0.00625	0.00004825
Division Range	13 - 1278	8 - 510	13 - 1278	8 - 1023	1 - 63	1 - 511
Power(mW)	3.23 @ 3.5 GHz	15 @ 2.5 GHz	3.58 @ 3 GHz	12 @ 2.5 GHz	0.62 @ 0.7 GHz	0.181 @ 1.25GHz
FOM (GHz/mW)	1.08	0.17	0.84	0.21	1.13	6.78

Table I shows the comparison between the results of previous work and the proposed programmable frequency divider using the same CMOS technologies. The Figure Of Merit (FOM) is used to compare the results,defined as the operation frequency of the circuit for each milli watt of power consumption (GHz/mW). The Results shows that the proposed frequency divider provides the lowest core area, power consumption, and highest FOM using a simple architecture. The power consumption and FOM of the proposed divider are 0.181 mW and 6.89, respectively. The proposed programmable frequency divider performance is compared with [3] and [11]. This work provides 50% duty-cycle output accurately. In Addition to this, the divisor range is greater than that of previous work and it can be easily extended to higher divisor ranges. For example, if a 10-bit asynchronous counter is employed, the divisor range will extend from 1 to 1023, realizing the design of full-division-range and low-area programmable frequency divider with a 50% duty-cycle output.

V. CONCLUSION

This brief presents a low area programmable frequency divider with standard cell layout design in 28nm technology with improved 50% duty-cycle output. The number of inputs for the proposed programmable frequency divider are increased and the area of the device is reduced by using standard layout technique. This design uses 0.9 volts power supply, it is operated with in 1MHz to 2GHz. The division ratio ranges from 1 to 511 at 1.25 GHz of input clock and output duty cycle ranges from 48.47 to 52.22. The total power consumption is 0.176 mW at 1.25GHz and active die area 0.000048204 mm^2.

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