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Implementation of Ternary Logic Gate

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Abstract: **-- A ternary logic system was first proposed by the polish mathematician Jan Lukasiewicz, in 1920.The ternary circuits developed are shown to have some significant advantages relative to other known binary circuits like low power dissipation, and reduced propagation delay and component count. Nevertheless, the associated reduction in the word length in the case of the ternary circuits tends to alleviate to a large extent the pin limitation problem associated with VLSI implementation. In this paper the basic gate implementation is considered and the power requirements for different methods of realization was studied.**

I. INTRODUCTION

The intrinsic switching behavior of many electronic devices makes them appropriate for implementing binary digital integrated circuits. Powerful arithmetic components and tools have supported binary logic over the last few decades to obtain the present status. However, the main disadvantages of the binary integrated circuits are interconnection and pin-count, cause limitations on the number of connections inside and outside of the circuit. One of the most effective solutions is to incorporate analog logic advantages in digital logic and consequently to deal with more data levels instead of just two, "0" or "1". This lead to the use of higher radices and consequently Multiple-Valued Logic (MVL) instead of binary logic, which resulted in decreasing the number of interconnections and pin-counts on a given chip

Ternary and quaternary circuits have been studied increasingly in recent years. Quaternary circuits have the practical advantage that a four-valued signal can easily be transformed into a two-valued signal. However, based on the following considerations, the ternary circuits may be of more theoretical significance than quaternary:

(a) Since 3 is the smallest radix higher than binary, ternary functions and circuits have the simpler form and construction. They can be studied and discussed easily, yet they still display the characteristics of multi-valued elements.

(b) As a measure of the cost or complexity of multi-valued circuits, the product of the radix and the number of signals has been proposed. Since 3 is the digit nearest to e = 2.718, ternary circuits will be more economical according to this measure.

(c) If balanced ternary logic (1, 0, - 1) is used, the same hardware may be used for addition and subtraction.

(d) Since 3 is not an integral power of 2, research on ternary logic may disclose design techniques that are overlooked in the study of binary or quaternary logic.[1].

Ternary based logic gives us new and exciting possibilities in gate design. The traditional binary based gate design gives us a single unary operator gate and three binary operator gates (with their corresponding negations. Whereas, ternary logic opens up a world of possibilities in unary, binary and ternary based input systems. Theoretically, MVL has the potential of improving circuit performance for applications, such as arithmetic and digital signal processing. Ternary based circuits are faster, require fewer operations, less gates, and signal lines. MOSFETs are used due to the fact that MOSFETs support three levels which are required for ternary. In section II .implementation of ternary is discussed in section III. Pros and cons of ternary logic are discussed. In sections IV through IX models of ternary inverter are discussed. Conclusions are presented in section X.

II.IMPLEMENTATION

In voltage mode operation of circuit, three distinct logic levels are defined in terms of voltage where as in current mode operation; states are integral multiple of reference current. Fig1 shows ternary levels in terms of voltage as low (V_L,), intermediate (V_1) & high (V_H). Low voltage level corresponds to logical state 0; intermediate to logic state 1 & high to logic state 2 respectively. The logical symbolism assumed is given in Table 1.

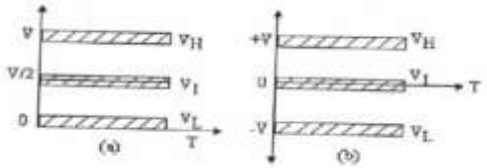

Fig 1: logic levels in ternary system : (a) when supply voltage is 0 to +v volt (b) when supply voltage is –v to +v volt

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(a) Supply voltage 0 to +V

Voltage level	Logic value
V	2
V/2	1
0	0

(b) supply voltage -V- to +V

Voltage level	Logic value
+V	2
0	1
-V	0

Table1:Logic symbol for ternary system

III. PROS AND CONS OF TERNARY LOGIC IN COMPARSION WITH BINARY LOGIC

- since each wire can transmit more MVL information than binary, the number of connections inside the chip can be reduced
- since each MVL element can process more information than a binary element, the complexity of circuits may be decreased
- The connections on- and off-chip can be reduced to help alleviate the pin-out difficulties that arise with increasingly larger chips
- The speed of serial information transmission will be faster since the transmitted information per unit time is increased.[1]

IV. SIMPLE TERNARY INVERTER (STI):

The first type of ternary inverter is the simple ternary inverter (STI). For the inputs {0, 1, 2} it yields the output {2, 1, 0}. Because of its ability to produce {1} at the output, STI is used as the primary building block for any design .A high resistance transmission gate is connected between the output of a low-resistance threshold modified binary inverter and 0.5Vs to produce the middle level voltage.[2] Sti with resistor is also designed in order to reduce transistor count.

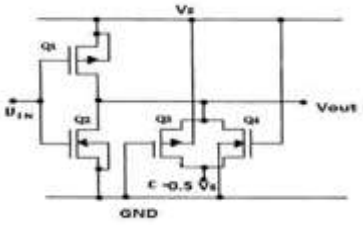

Fig 2: Transistor schematic of STI

V. NEGATIVE TERNARY INVERTER (NTI):

The Negative Ternary Inverter (NTI) was implemented using the same logic designs and sizing requirements for the input of {0, 1 and 2}, NTI provides the output {0, 0, 2}. An always on transistor (NMOS for NTI) is used for the passing the middle voltage instead of a transmission gate.[2]

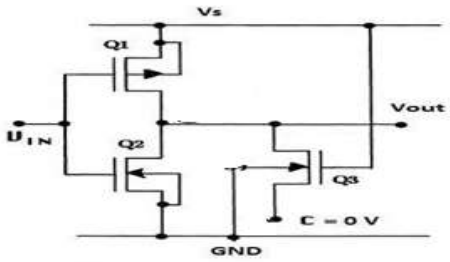

Fig 3: Transistor Schematic of NTI

VI. POSITIVE TERNARY INVERTER (PTI):

The Positive Ternary Inverter was implemented using the logic design and sizing requirements an input of {0, 1, 2} provides {2, 2, 0} for output of PTI. In PTI, an additional always on transistor (PMOS for PTI) is used to pass middle voltage. As the design of PTI and NTI is more of a very – high skew (PTI) or very low-skew (NTI) binary inverter rather than ternary inverter, their speed of operations is much faster than the STI. These inverters were useful in creating the precoder logic, and in helping to differentiate the trit TL logic levels.[2]

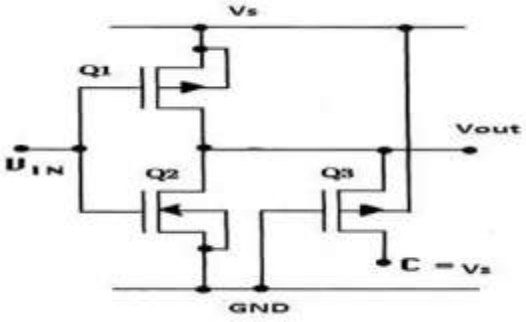

Fig 4: Transistor Schematic of PTI

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VII. INVERTER CIRCUIT OPERATION (DYNAMIC):

The circuit realization of the STI: when *pre* is high, the gate is precharged at the *V*I level, whereas the inverter evaluates the input value when *pre* is low. The behavior of these gates is strongly dependent on the choice of the supply voltages *VDD* and *VSS*, the logic levels *V*H (high), *V*I (intermediate) and *V*L (low), and on the technological process parameters (e.g., the threshold voltages): in particular, the body effect on the NMOS and PMOS.Transistors determines the actual switching threshold.[3]

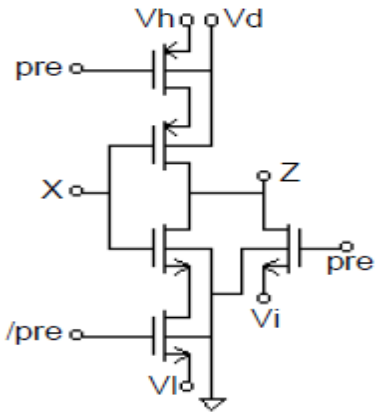

Fig 5: Ternary inverter.

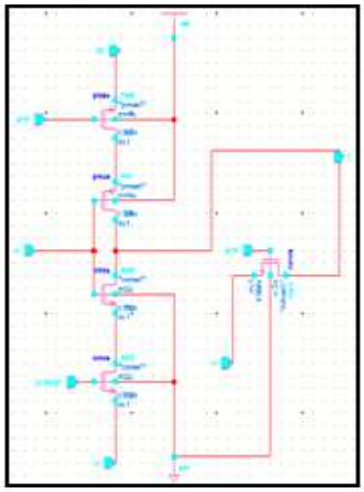

Fig 6: STI Dynamic Schematic

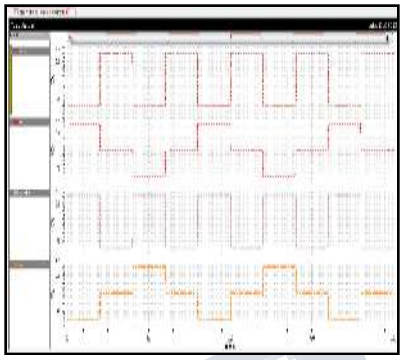

Fig 7: Waveforms Dynamic Of Inverter

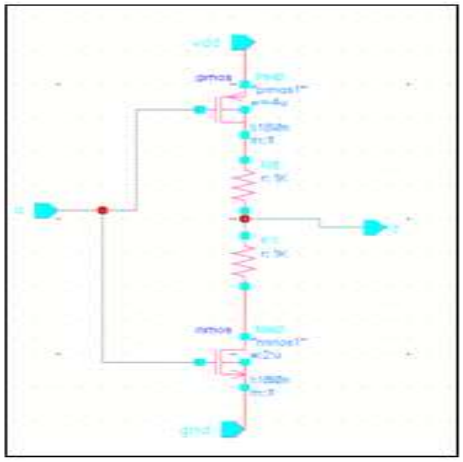

Fig 8: STI With Resistor

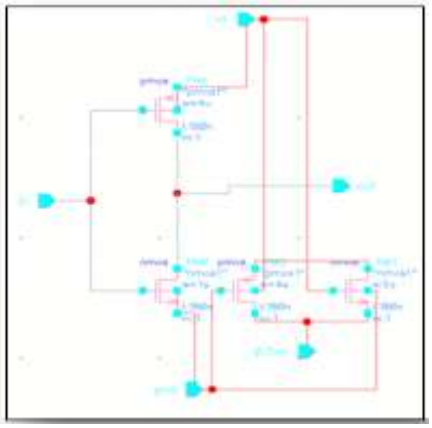

Fig 9: STI without Resistor

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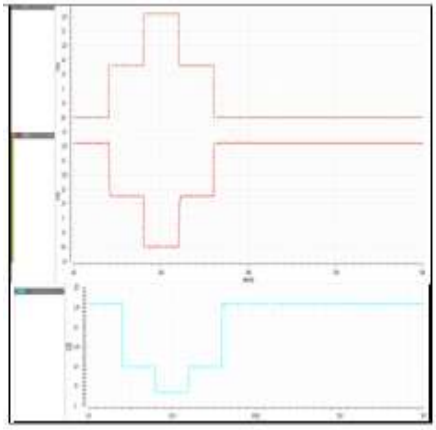

Fig 10: Output Waveforms Of STI With And Without Resistors

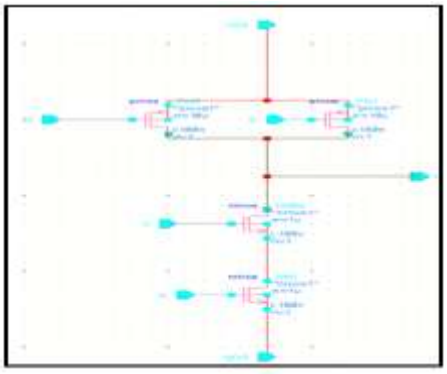

Fig 11: Ternary Positive Nand

Fig 12: Ternarynegativenand

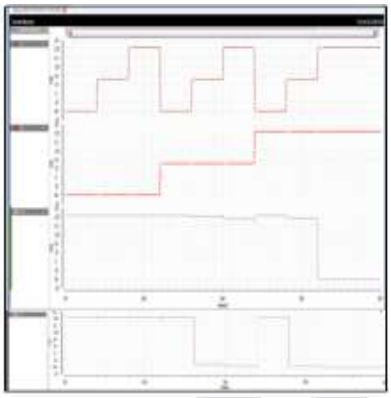

Fig 13: Output Waveforms Of Ternary Positive And Negative Nand

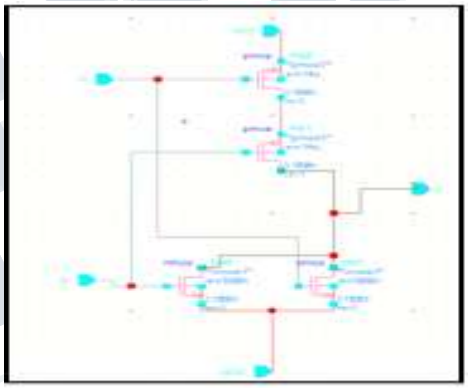

Fig 14: Ternarypositivenor

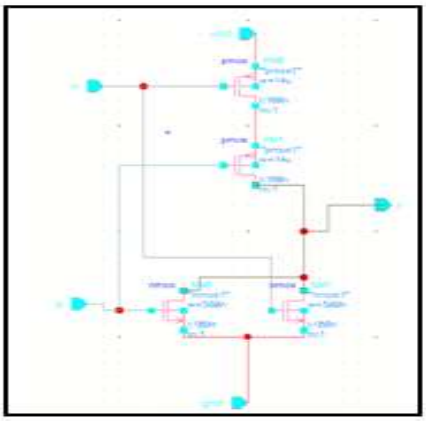

Fig 15: Ternarynegativenor

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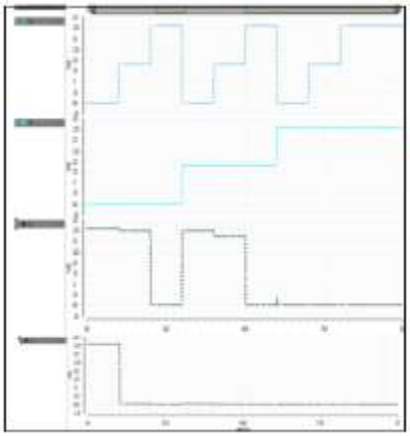

Fig 16: Output Waveforms Of Ternary Positive And Negative Nor

VIII .TRANSISTOR COUNT

Inverter		Nand		Nor	
Circuit	count	Circuit	count	Circuit	count
STI without resistor STI with resistor STI dynamic	4 2 5	Ternary positive Nand Ternary negative Nand	4 4	Ternary positive Nor Ternary negative Nor	4 4

IX. POWER

Inverter		Nand		Nor	
Circuit	Power	Circuit	Power	Circuit	power
STI without resistor STI with resistor STI dynamic	7.283512e-13 0.0015927596 1.0269298e-04	Ternary positive n and Ternary negative n and	2.8662829e-11 1.8153739e-11	Ternary positive nor Ternary negative nor	1.2141269e-9 5.9437316e-11

X. CONCULSION

Considering the various advantages of the ternary, the appropriate design of ternary logic gates is important so that it will lead to the further development and its application in VLSI.

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