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Design and Realization of Low Power Multiple Sensors Node & its VLSI Implementation

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Abstract: **-- The sensor intelligence has been emerged with a low power processor model. Sensor node within single chip has been developed and implemented on a high performance FPGA kit. This paper is for the purpose of designing a FPGA based data acquisition system, utilizing the high processing speed feature of FPGA The FPGA data acquisition module is designed by the VHDL and simulated by the ISE software. This system has the advantage of being a simple unit with low power consumption and being used to collect data from different sensors. In proposed System, FPGA can sense the maximum of 8 analog channel input from ADC. After conversion of analog to digital. No need to store the corresponding digital data with external memory. You can able to store the digital data in FPGA embedded RAM itself and also the Stored digital data in Xilinx Platform PROM (XCF01S).So that digital data is not erased, until again reprogramming the FPGA ic. The prototype is implemented in SPARTAN-3E FPGA board and coding used is VHDL.**

Keywords: **-- analog to digital conversion, data acquisition, sensors, FPGA.**

I. INTRODUCTION

Moore's law which states that the "number of transistors that can be placed inexpensively on an integrated circuit will double or so for every two years," has been the main focus of subsequent criticism;

While it boldly states the consent of technology scaling. An immediate outcome of Moore's law is that the "power density of the integrated circuit will increase exponentially with each technology generation". History is witness to this particular incontrovertible fact that this is not a begin outcome. This implicit trend has debatably led to some of the foremost vital and important changes in electronic and computing changes.

For high performance VLSI chip-design, the choice of back-end methodology incorporates a significant impact on the design time and price. Making each single gate from scratch isn't essentially the simplest method. Despite, an adequate set of predesigned standard cells are often utilized as building blocks to design most of the functional blocks. Semiconductor manufacturers supply standard cell libraries that also are supported by CAD tools in automated design flows together with the ultimate physical auto-placement and routing.

Electronic design automation

Electronic design automation (EDA or ECAD) is one of the major category software tools electronic systems for designed such as integrated circuits and printed circuit boards. For many years, the larger electronic companies, such as the two names of Hewlett Packard, Tektronix, and Intel, had trailed EDA within. In 1981, managers and developers gyrated out of these companies to concentrate on EDA as a business. The low power performance has been a vital role in the VLSI systems of any circuits and design and the main intension is also to reduction of the power.

II. PROPOSED SYSTEM

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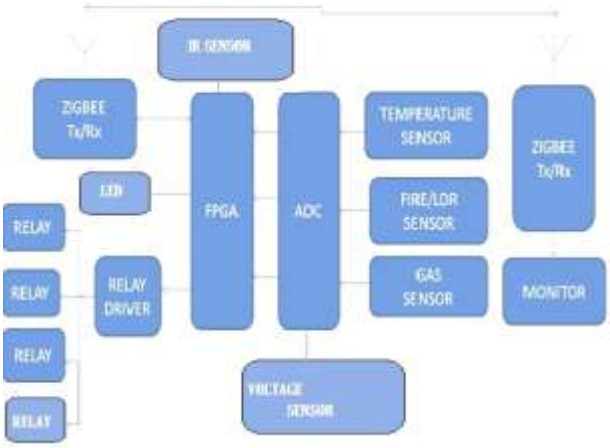

Fig.2.1. Project Block Diagram

- Temperature sensor : Detect the temperature from the industry.
- Fire/LDR sensor : Light Dependent Resistor Detect the fire.when ever fire accident is occur in industry.
- Gas sensor: Detect the harmful gases fromfactory(CO,NO2,SO2..etc)
- Voltage sensor :Detects the voltage levels of the sytem
- IR sensor: Detects the objects/obstracles in nearer to it.
- ADC : Analog to Digital Converter
- FPGA:Field Programmable Gate Array

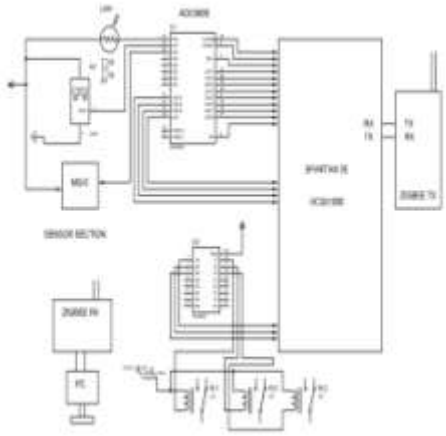

Fig 2.2: Interconnection diagram

In proposed system ,FPGA can sense the FOUR channel input from multi channel ADC.After coversion of analog to digital no need to store the corresponding digital data with external memory.we can able to store the digital data in FPGA embedded RAM itself and also the stored digital data in Xilinx platform PROM(XCFO1S).so that digital data is not erased ,until again reprogramming the FPGA IC.

Basic Operation

Here I can use five sensors always sensing the environmental condition in chemical factory and if any abnormal change in environment.then the sensor will give the analog input to multichannel ADC.then ADC will covert analog signal from sensors into digital value.here the FPGA will operate on the digital value i.e.if temperature value is higher than 40 degree celsius means ,the FPGA will turn on the alaram,which is interfaced with FPGA.

Here the fire/LDR sensor can be used for detect the fire accident.when ever fire accident is occur intensity of the light is very high.with the help of LDR it is easy to find out the fire accident .if we are implementing this cocept for the industries ,it is very useful to indicating fire accidents.

In this project I can use the gas sensor for detect the harmful gases from the chemical factory.if gas value is higher than 50 PPM means ,the FPGA will turn on alaram ,which is interfaced with FPGA.We can see the sensor's analog waveform in application soft ware and also we can set the the threshold value for all sensors manually in that application software.

Advantages

- Low power consumption.
- Easily identify the high temperature, gas and fire from the industries so that the preventive action can be taken immediately.
- Easy to handle and operate the equipment
- Low maintenance cost
- High processing speed and high accuracy, storage and portability.

Applications

- Industrial automation and monitoring purpose
- Medical equipment monitoring
- Military application
- RF communication

III. TOOLS REQUIRED:

Software Tools:

1. Xilinx
2. VB software

Hard ware Components

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a) Power Supply
b) Analog To Digital Converter
c) Zigbee Module
d) DB9 Connector
e) Xilinx Spartan -3E FPGA Board
f) Sensors (Temperature, Gas ,LDR ,Voltage ,IR Sensors)
g) Relays
h) LAN Network

IV. IMPLEMENTATION

Hard ware implementation of ic

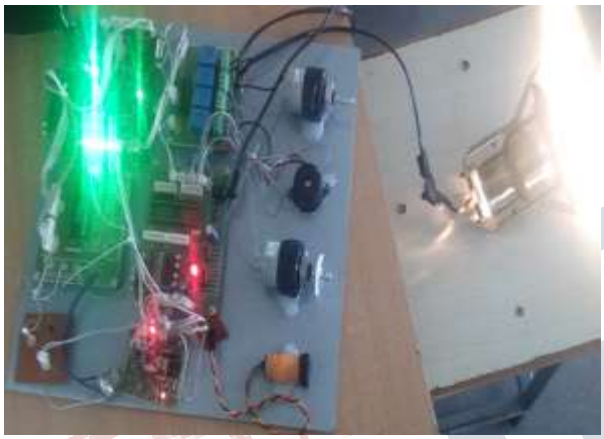
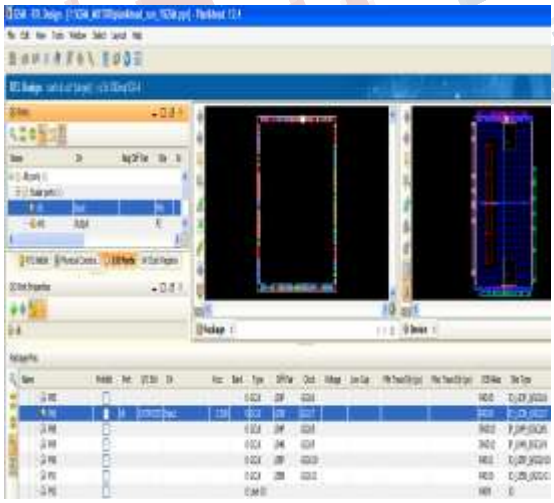


Fig 4.1: Multiple sensor node implementations

Assigning pin location constraints



Pin location for all the ports of proposed multiple sensor node are specified so that all available pins are connected on FPGA kit efficiently. Total regarding information concerned to the pin locations was saved in UCF file. Xilinx window contains all information. The UCF file is created in that assigning pins to all the ports of 0808ADC. The acronym of UCF is user constraint file. During the simulation process UCF file is created. It consisting of all the pin numbers and assigning location based on this, the pin acts and stores all the information. After simulation process takes the hard ware part execution is done, finally the analog signal is converted in to digital signal. The Xilinx face window contains device architecture and package pins for device Spartan 3 series. Here, the Spartan 3E board is used and the implementation takes.

V. RESULTS

Simulation Results

5.1 RTL (Register transfer level) schematic

RTL stands for register-transfer level and its abstraction is used in hardware description languages to create high-level representations of a circuit, from which lower-level representations & ultimately actual wiring can be derived. The below figure shows register transfer level schematic.

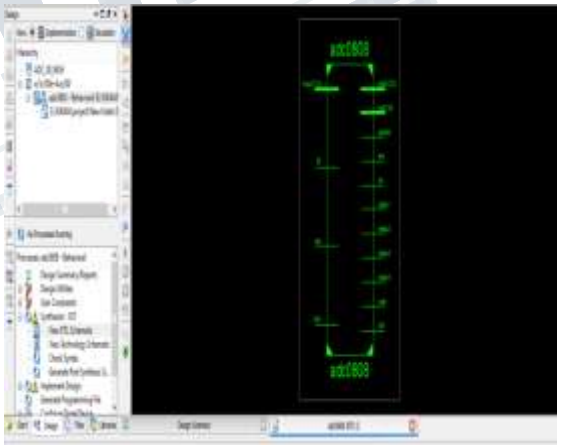


Fig 5.1: RTL schematic

5.2 Technology schematic

The technology schematic is shown in below figure 5.2.It consisting of inner sub modules of the register-transfer level blocks. It gives each sub blocks schematic of main register level main module. In this number of gates used as logic levels, number of LUTs used all things shown in this technology of 0808 ADC and FPGA file also generated.

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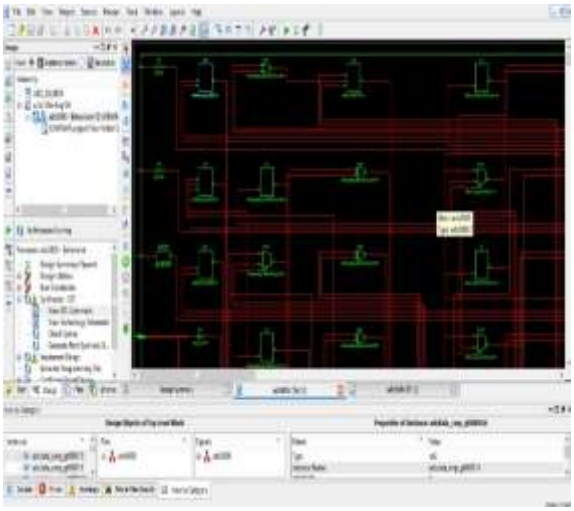


Fig: Technology Schematic

5.3 Simulation analysis of proposed method

The address lines add[2:0] specifies the sensor to be activated .The data acquisition from the sensors is done parallely and the each address line stores the respective sensor outputs. The data to the address lines will comes from ADC0808.if the sensor output is exceed the set point then the relay will be activated automatically.in this project we used IR Sensor[digital sensor]it is connected directly to the FPGA board .fpga will get digital data directly .so,there is no need of converstion for IR sensor.if any object diteted by the IR SENSOR then the controller connected to IR sensor will be putoff.in simulation output the relay4 will ON when the IR sensor input is

1

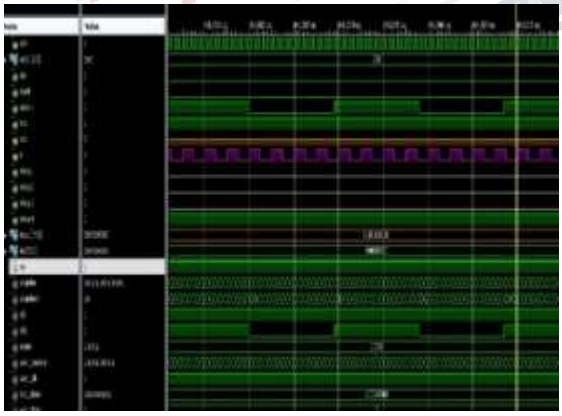


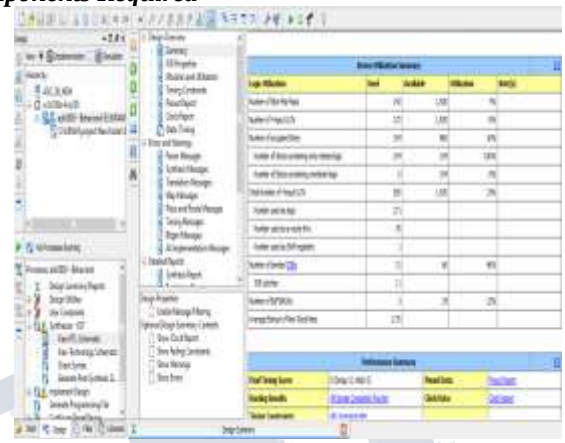
Fig: Timing waveform

Analysis Report:

Total delay=gate delay + net delay

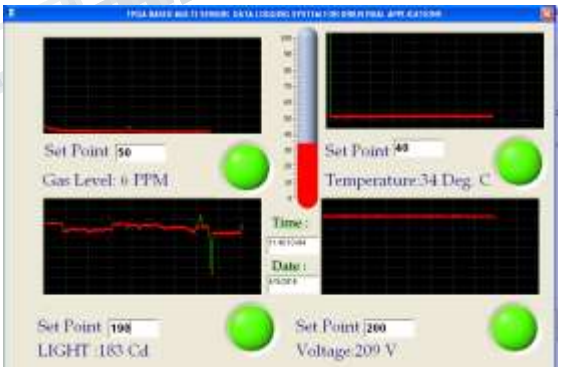
Delay: 5.048ns (Levels of Logic = 2)
Proposed power optimization: 30uw

Components Required



The above figure shows clearly how many gates used and flip-flops and look up tables. This summary gives whole information regarding the concerned projects. Number of BUFGMUXs and number of inputs all the things shown. Mainly UCF file is created after this table shows gates how many used.

VB OUTPUT



It is user friendly software tool that shows the sensor outputs in the monitor of the screen.

VII. CONCLUSION

This proposed FPGA based multiple sensor node system is designed for industrial automation. The system is integrated with multiple sensors, and we will store the digital data from sensors in internal RAM on the FPGA board. So, no need of external memory. By this multiple sensor node the

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area optimization is done, delay occurred is very less & less power optimization. Advantage of using FPGA is also due to its reconfigurable feature without changing the hardware itself.

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BIOGRAPHY

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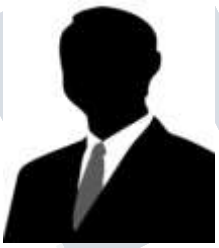

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