ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronic and Communication Engineering (IJERECE)
Vol 3, Issue 7, July 2016

ASIC Implementation of 32-bit MIPS RISC Processor using Multi-VDD Technique

[1] Jeyakumar R,[2]Suryavanshi Rushank Sharad [3] David Jey Singh[4] Jayakrishnan P
[1][2][3] M.Tech –VLSI Design, [4] Assistant Professor (Senior)
[1][2][3][4]School of Electronics Engineering (SENSE), VIT University, Vellore-632014
[1] r.jeyakumar23@gmail.com [2] srushank@yahoo.com [3] davidjeysingh@gmail.com
[4]pjayakrishnan@vit.ac.in

***Abstract*— the phenomena of scaling down the device results into certain hazards in the processor However it can have an adverse impact on the various performance parameters of the processor as area, power and timing. However in order to overcome the enlisted shortcomings the design of Microprocessor without Interlocked Pipeline Stages (MIPS) architecture is preferred. The Microprocessor without Interlocked Pipeline Stages is a RISC processor. The architecture discussed is implemented using Verilog HDL. Further ASIC flow is performed using 32nm technology. However low power realization is achieved by using multiple voltage (Multi-VDD) technique where by the critical path in the design is analyzed and the voltage of that respective path is increased there by achieving a good speed up.**

***Keywords*— Technology; Instruction Set; MIPS; Pipeline; RISC; Verilog HDL**

I. INTRODUCTION

CISC remains for Complex Instruction Set Computer. The primary point of CISC design is to finished an assignment in as few lines of guideline as could be allowed. CISC Instruction characteristics are, it has countless set, Complex and broad directions, Extensive control of low-level computational components for memory, double number juggling and tending to, Efficient small scale encoding of machine guidelines also, Processor substance moderately less registers. Due to complex engineering of CISC, every guideline takes more time to execute, including less complex directions. Framework 360– IBM, VAX– Digital Equipment Corporation, PDP-11–Digital Hardware Corporation, Motorola 68000 family and Intel x86 engineering processors utilizes the CISC design.

RISC remains for Reduced Instruction Set Computer. The fundamental point of RISC design is to create a more straightforward and quicker arrangement of directions. RISC design is created as a response to CISC. Guidelines of RISC ought not take as long to keep running as this is the drawback to CISC plan. RISC gives software engineers with less difficult directions that can execute rapidly. RISC traits are, it substance a littler number of directions, Instructions can execute in one machine cycle or less, Encoded directions are the same size and engineering contains numerous registers which are sorted out into register document.
Basic directions permit RISC processor to be less demanding to outline and less expensive to create. It requires less number of transistors permitting the processor to be littler. It is simpler to make effective enhanced compilers since there are less directions in the guideline set. Macintosh iPods, iPhone, iPad, Palm and PocketPC, PDAs and Smartphones utilizes RISC design.

MIPS Technologies has a solid client licensee base in home hardware and compact media players; 75 percent of Blu-beam Disk players are running on MIPS Technologies processors. In the advanced home, the organization's processors are predominately found in computerized TVs and set-top boxes. The Sony PlayStation Portable uses two processors taking into account the MIPS32 4K processor. Inside the systems administration section, licensees incorporate Cavium Networks and Net rationale Microsystems. Licensees utilizing MIPS to construct advanced cells also, tablets incorporate Actions Semiconductor and Ingenic Semiconductor. Tablets in light of MIPS incorporate the Cruz tablets from Velocity Micro. TCL Corporation is utilizing MIPS processors for the advancement of PDAs. Organizations can likewise get a MIPS building permit for outlining their own particular CPU centers utilizing the MIPS guideline set. MIPS

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronic and Communication Engineering (IJERECE)
Vol 3, Issue 7, July 2016

Innovations is predominately utilized as a part of conjunction with Android and Linux working frameworks. Thus, planning of RISC Processor in light of MIPS Instruction set is the essential decision.

The paper is organized into the following sections. Section II explains about the literature review. Section III explains about the architecture of MIPS . Section IV explain the simulation results and Section V explains the low power approach and Section VI explain the conclusion and Results

II. LITERATURE SURVEY

P.V.S.R Bharadwaja, KRavi Teja, M. Naresh Babu, K. Neelima have proposed that [1] as the technology node scales down the scope of undesirable hazards in the processor greatly increases. This may lead in deviation from desired parametric values of area, power and timing of the system. The enlisted shortcomings can be overcome by Microprocessor without Interlocked Pipeline Stages which is a recent architecture.S. P. Ritpurkar, M. N. Thakare, G. D. Korde, have proposed that [2] the processor is analyzed on basis of Instruction fetch module, Decoder module, Execution module which includes 32Bit Floating point ALU, Flag register of 32Bit,MIPS Instruction Set, and 32Bit general purpose registers and design theory based on 32Bit MIPS RISC Processor. Here in the concept of pipeling involves Instruction Fetch, Instruction Decode, Execution, Memory and Write Back modules of MIPS RISC processor based on 32Bit MIPS Instruction set in a single clock cycle. Mohit N. Topiwala and N. Saraswathi have proposed that [3] a MIPS processor that can be implemented using HDL. A RISC is a microprocessor that had been designed to perform a small set of instructions, with the aim of increasing the overall speed of the processor. MIPS have 5 stages of pipeline viz. Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory Access (MEM) and Write Back (WB) modules. Mazen Bahaidarah, Hesham Al-Obaisi ,Tariq Al-Sharif , Mosab Al-Zahrani [4] and Xizhi Li, Tiecai Li, [6] have proposed the implementation of processor architecture on FPGA that has become a renowned methodology for application specific customization. In the similar aspects the implementation of MIPS 32 bit processor can be carried out on suitable FPGA. Shuai Wang, Yang Li, Junbao Liu, Jun Han have proposed [5] the implementation of MIPS processor that can be extended to realize certain applications. As an example certain encryption related applications like AES and ECC algorithms are of focus regarding the implementation aspects are concerned. Also functionality as well as throughput are of prime importance. B. Zivkov, B. Ferguson , M. Gupta have proposed [7] the desired MIPS R4200 for low power and low cost. It is capable of powering a notebook, portable devices, and low cost desktop systems running on Windows NT or UNIX.

III. MIPS INSTRUCTION SET ARCHITECTURE

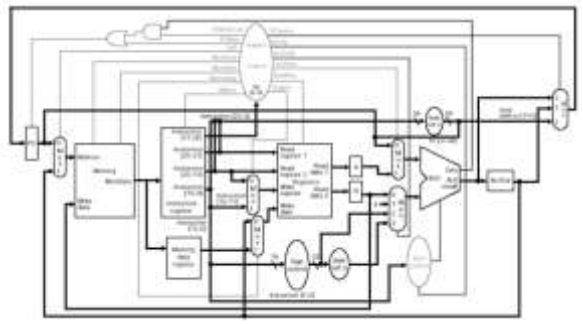

Fig. 1. MIPS Architecture

The architecture is broadly classified into Data path and Control Unit. Data path provides a path for the instructions and data through the processor. The components are connected by buses. In MIPS the bus width is usually 32 bits. The major components of the data path are Program Counter, Instruction Register (IR), Register file, Arithmetic and logic unit (ALU) and Memory. In MIPS, programs are separated from data in memory. MIPS have two segments Text Segment and Data segment.

MIPS based RISC processor is fundamentally pipe lined engineering execution. MIPS engineering conveyed 5 phases of pipeline. Pipelining is only accomplishing more than one operation, in a solitary information way. Pipelining is a strategy which is utilized to enhance general execution of RISC processor [7]. A multicycle CPU comprises of numerous procedures. For instance burden may take up to 5 clock cycles, yet beq takes just 3 clock cycles. So in the event that one procedure is occurring, rather than sitting tight for the procedure to finish, all the while begin another procedure in the same information way, without exasperating the past procedure. For this to happen, the every part of the procedure is partitioned into different pipelined stages. So after each clock, the procedure is put away into next channel lined stage, empowering another operation to begin in that stage without irritating the past procedure. Henceforth all the stages in the way can be

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronic and Communication Engineering (IJERECE)
Vol 3, Issue 7, July 2016

utilized at the same time. This thus can expand the throughput of MI PS plan.

MIPS processor architecture has been implemented using 5 pipeline stages. These pipeline stages are Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory Access (MEM) and Write Back (WB).

IV. SIMULATION RESULTS

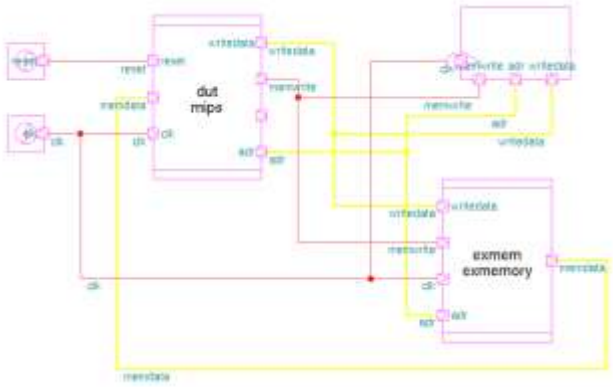

Fig. 2. MIPS Architecture RTL Schematic

The RTL schematic for the designed MIPS processor is as shown in the Fig.2. The schematic comprises of a MIPS processor and an external memory access. The MIPS processor has sub-modules namely, the controller module, data path element and alu control module. The detailed diagram for the MIPS processor is as shown in the Fig.3.

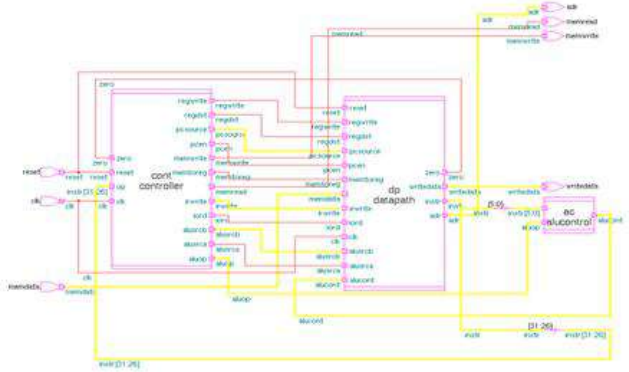

Fig. 3. RTL schematic of ALU

As seen from the figure the datapath is the path between the instructions and data through the processor. The controller unit controls the components of the datapath that are required for execution cycles. The synthesis is performed using 32nm library and subjecting to constraints of area, power and timing. The library used for synthesis is saed32hvt_ff0p85v25c. The layout of the MIPS processor after the entire ASIC flow is as shown in the Fig 4. The synthesis results for area, power and timing for the MIPS processor are summarized in the table I.

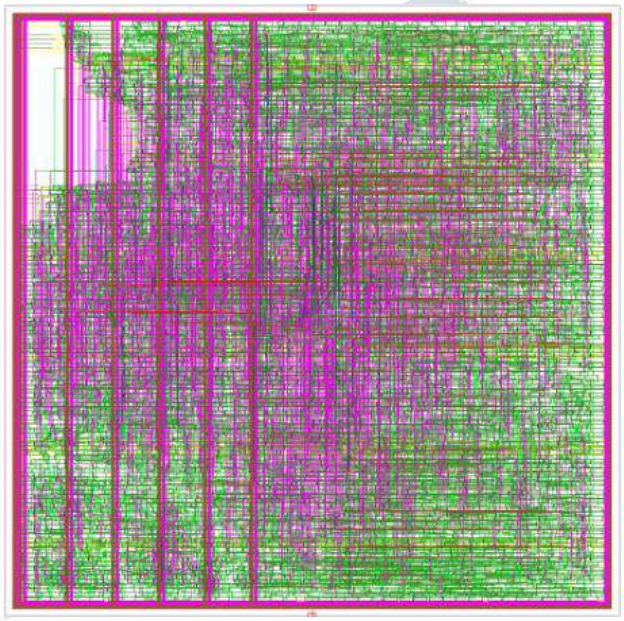

Fig. 4. MIPS architecture after ASIC implementation.

TABLE I . SYNTHESIS REPORT

Area (sq.microns)		Power (mW)		Timing (ns)
Before Constraints	After Constraints	Before Constraints	After Constraints	After Constraints
110886.63	121156.09	19.297	3.3168	1.70

V. THE LOW POWER APPROACH

In order to achieve the low power reduction for the desired architecture, the approach of multiple voltages (multi-VDD) is used. The approach for the architecture is explained as follows. Consider the RTL schematic for the MIPS processor as shown above. From the schematic it can be predicted that the controller module has to perform faster operations since it is involved for synchronizing the transfers between the processors and the external memory

interface and also the transfers can consume a considerable amount of time.

Hence as per the multiple voltages approach the module one which has high computation time, the voltage should be increased as it is in the critical path of the design or architecture. The high voltage used for the module is 0.95V and low voltage used for the modules is 0.7V. So as per the stated reason the voltage of controller is scaled to higher level where as the elements or the modules which are in non-critical path are scaled to lower voltage levels. This approach is obtained by sourcing Universal Power Flow (UPF) file. So in this approach of low power reduction the power obtained without subjecting to constraints is 19.297 mW whereas on following multiple voltage approach by sourcing the universal power flow file the power reduces to 3.3168mW there by achieving the goal of low power design for the architecture.

VI. CONCLUSION:

Thus the design of MIPS processor is achieved using Verilog-HDL. The various modules like processing unit, datapath and controller modules are designed using the same hardware description language. Further logical and physical synthesis is performed using 32nm library(saed32hvt_ff0p85v25c). The design is subjected to area, power and timing constraints for achieving the entire ASIC flow. The processor working of processor is facilitated at the operating frequency of 1000 MHz with a slack of 1.70 ns. In order to achieve the low power realization for the architecture multiple voltage technique is used where in the critical path is analyzed and the voltage of modules in that path is raised. It is observed that power without this approach is 19.297 mW but on subjecting to the constraints it reduces to 3.3168m W there by showing a 15.98 mW significant power reduction.

REFERENCES

[1] P.V.S.R Bharadwaja, KRavi Teja, M. Naresh Babu, K. Neelima, "Advanced low power RISC processor design using MIPS instruction set", 2nd International Conference on Electronics & Communication Systems, pp.161-167, Feb 2015.

[2] S. P. Ritpurkar, M. N. Thakare, G. D. Korde, "Synthesis and Simulation of a 32Bit MIPS RISC Processor using VHDL", International Conference on Advances in Engineering and Technology Research (ICAETR), 2014.

[3] Mohit N. Topiwala , N. Saraswathi," Implementation of a 32-bit MIPS based RISC processor using Cadence, International Conference on Advanced Communication Control and Computing Technologies (ICACCCT)", 2014.

[4] Mazen Bahaidarah, Hesham Al-Obaisi ,Tariq Al-Sharif , Mosab Al-Zahrani, "A novel technique for run-time loading for MIPS soft-core processor", Electronics, Communications and Photonics Conference (SIECPC), 2013.

[5] Shuai Wang, Yang Li, Junbao Liu, Jun Han , "A security processor based on MIPS 4KE architecture, IEEE 9th International Conference on ASIC (ASICON)", 2011.

[6] Xizhi Li, Tiecai Li, "ECOMIPS: an economic MIPS CPU design on FPGA", 4th IEEE International Workshop on System-on-Chip for Real-Time Applications, 2004.Proceedings, 2004.

[7] B. Zivkov, B. Ferguson , M. Gupta, "R4200: a high-performance MIPS microprocessor for portables", Compcon Spring '94, Digest of Papers,1994.