International Journal of Engineering Research in Electronic and Communication Engineering (IJERECE) Vol 3, Issue 5, May 2016

A 90NM Low Power Ota Using Adaptive Bias

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***Abstract*— Low power class AB operational trans-conductance amplifier (OTA) which is fully differential operating at low voltage 0.4 V supply designed in low cost 90nm technology is proposed in this paper. Differential pairs such as P channel and N channel with complementary input configuration are used in input stage to achieve input common mode range (ICMR) which is full rail to rail. For increasing slew rate without sacrificing power consumption adaptive bias circuits are used hence amplifier works in class AB. The common mode feed forward circuit (CMFF) is employed for maximizing common mode rejection ratio (CMRR). To make system power efficient whole amplifier operates in weak inversion region. After designing layout of an op amp, Simulation with parasitic is carried out and shows that DC gain of 51.15 dB, 876.5 kHz unity gain bandwidth (UGB)with 77.7° phase margin for 10 pF capacitive load and slew rate of 0.1 V/µs; CMRR and PSRR are 116.9 and 97.30 dB respectively. The proposed OTA dissipates very less power of 4.78 µW and shows ability to use in applications where less energy is mandatory.**

***Keywords*- Adaptive bias, class AB, CMFF, CMRR, ICMR, OTA**

I. INTRODUCTION

In current days popularity of portable battery powered equipment is growing that diverts analog circuit designer area of interest towards low power integrated circuit (IC) design. To accomplish designing task of IC consuming less power needs to reduce supply voltage, and parasitic (resistance, capacitance, inductance and bipolar transistor) generated among the whole layout of an IC is minimum. In Analog circuits, transistors operating in weak inversion region dissipate less power but operate slowly. Hence performance achieved in this region is suitable for applications in which less energy required and saving energy is their primary target, while most of the times we might have to sacrifice speed and dynamic range [1]. In modern integrated systems, Operational amplifier operates as a most essential block and largely used in a circuit topologies like filters, voltage regulators and data converters, etc [2]. The layout designing and post layout simulation are most important steps in IC design process. Layout is a representation of circuit using various layers (metal, well, oxide, etc.). Improperly designed Layout of an IC adds parasitic that affect circuit performance parameters. To avoid those parasitic and make area efficient Layout, there is a need to break transistors having higher width into multiple numbers to minimize gate resistance and area. While transistor pairs (current mirror and differential pair) also need to match to avoid mismatches due to process variation by using various matching techniques such as Inter digitized and common centroid.

The parallel arrangement of N channel and P channel differential input pair can be employed to extend ICMR from rail to rail. To avoid tradeoff between slew rate and power consumption, adaptive bias circuit with class AB output stage can be employed. CMFF circuit is more compatible for low voltage applications than Common mode feedback (CMFB) circuit [1]. The rail to rail voltage range of output stage can be fall narrow because of the Conventional common drain class AB configuration at output stages. To overcome this issue, output transistor in rail to rail stages of output should be connected in classical configuration such as common source [3]. Low power supply voltage makes single ended circuits very difficult to perform optimally hence fully differential circuits are used which improves output swing, linearity and CMRR [4]. Adaptive bias method of two level shifter (TLS) is better than winner take all (WTA) method because TLS method gives doubled transconductance to the input stage which boost the gain and unity gain frequency [5]. To address the above, low power CMOS OTA which is fully differential is proposed in this paper. This newly designed OTA provides excellent gain of 51.15 dB with improved UGB. It also avoids limitation on slew rate without sacrificing power consumption. Power consumption of the proposed OTA at 0.4 V supply is only 4.78 µw.op- amp is designed and simulations are carried using H- SPICE.

II. PROPOSED AMPLIFIER

2.1 Existing Amplifier

Fig.1 push-pull op-amp with current replication branch M2R and MoNR. Class AB operation is achieved by including an adaptive load at the input stage as shown in Fig.2 and Fig.3 which will be named adaptive load II and I respectively.

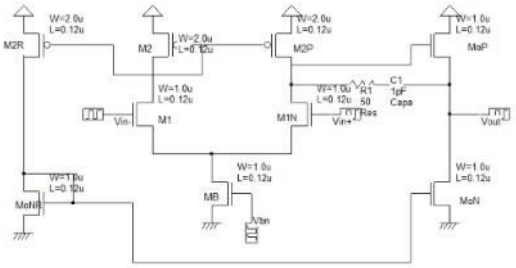


Fig.1.push-pull op-amp with current replication branch M2R, MoNR

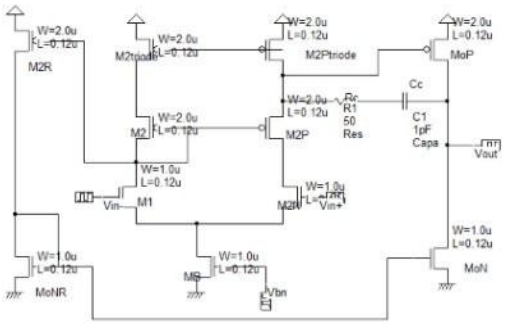


Fig.2.class AB two-stage op-amp with current replicating branch using adaptive load II at the input stage

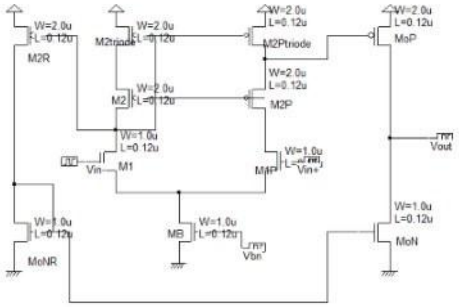


Fig3 .class AB two-stage op-amp with current replicating branch using adaptive load I at the input stage

In both cases, the adaptive loads exploit the large variation of output resistance of transistors *M*2triode-*M*2Ptriode between triode and saturation regions. Bias voltag sets these transistors at the boundary between triode and saturation regions in quiescent conditions. With both schemes, a current increase in *Ia* or *Ib* causes transistors *M*2triode or *M*2Ptriode to go in triode mode and to develop large drain-source voltages. These changes cause large variations at nodes **a** and **b,** which lead to large currents at the output with the increase in the slew rate without sacrificing the functionality of the circuit and hence power dissipation is also reduced.

2.2 Proposed O pamp

The proposed structure of op-amp consists of 3 main blocks. (a)The first block is input differential amplifier; it provides very high input resistances, a high CMRR and PSRR, and high gain with a low noise. Its output should preferably be single ended, so that the rest of the op-amp need not contain symmetrical differential stages. Since the transistors in the input stage operate in their saturation regions there is an appreciable dc voltage difference between input and output signals of the input stage.

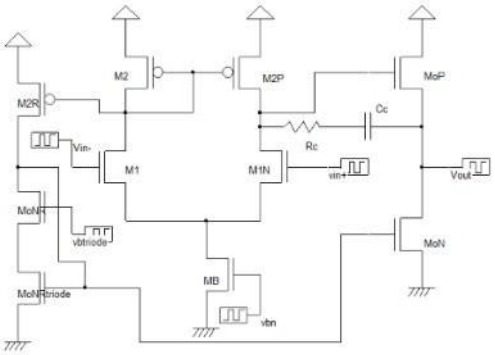


Fig4.proposed amplifier

(b)The second stage performs one or more of the following functions:

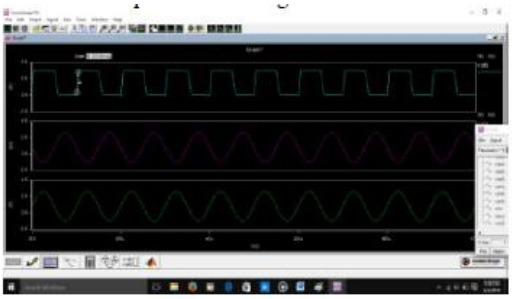
Level shifting: This is needed to compensate for the dc voltage change occurring in the input stage, and thus to assure the appropriate dc bias for the following stages. Added Gain: The gain provided by the input stage is not sufficient and additional amplification is required. Differential to single ended conversion: In some circuits, the input stage has a differential output, and the conversion to single ended signals is performed in a subsequent stage.

(c) The third block is the output buffer. It provides the low output impedance and larger output current needed to drive the load of the op-amp. It normally does not contribute to the voltage gain. If the op-amp is an internal component of a switched-capacitor filter, then the output load is a capacitor, and the buffer need not provide very large current or very low output impedance. However if the op-amp is at the filter output, then it may have to

drive a large capacitor current mirror and differential amplifiers and the common source amplifier and/or resistive load. This requires large current drive capability and very low output impedance which can only be attained by using large output devices with appreciable dc bias currents.

III. RESULTS AND DISCUSSION

From below table and simulation results we can see that the power is sufficiently and slew rate increased compared to existing circuits.



SCHEMATICS	Slew rate(v/us)	Power uw
Push pull op-amp with current replication branch	4.29	2.23
Class ab two stage op-amp with current replication branch and adoptive loads	7.83	2.13
Class ab two stage op-amp with current replication branch using adoptive load I at the input stage	7.9	2.03
Proposed OTA	8.09	1.46

IV. CONCLUSIONS

Proposed OTA working at low 0.4V supply voltage increases battery lifetimes and decreases number of batteries requires by the system for active operation while reduction in CMOS technology to 90nm consumes less area and make. For future work, addition of gain enhancement stages or implementation of gain improving techniques may boost gain of proposed.

Acknowledgement

I am thankful to his Holiness Poojya Dr.Sharanabaswappa Appa, Mahadasoha Peethadhipati, sharanabasaweshwar Vidhya Vardhak Sangha, Gulbarga and also thankful to principal and Dean ,AIET Kalaburgi.

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