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Low Power Flip Flop Implemented Using Transmission Gates and Feed through Logic

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***Abstract*— in this paper, a low-power flip-flop (FF) design featuring an explicit type pulse-triggered structure and a modified true single phase clock (TSPC) latch based on a signal feed-through scheme is presented. This paper solves the long discharging path problem in conventional explicit type pulse-triggered FF (MHLFF) design. An advanced simulation which targets to achieves better speed and power performance. Reducing redundant switching activity has a good impact on reducing power dissipation. CMOS 90nm technology have been used to implement simulation results. The maximum power saving is achieved as compared to the previous design. H-SPICE tool is used for simulation purpose.**

***Keywords*- Flip-Flops (FF), power consumption, transmission gate (TG), conditional pulse, low power, Low power dissipation.**

I. INTRODUCTION

An efficient design technique for the flip flop is required because flip flop are the most important components of the circuit which determines the overall performance of the circuit, correct timing performance of the entire circuit. For the improvement in the flip flop design three factors are to be considered area, power and delay factor. This paper presents a low power conditional pulse control with transmission gate flip-flop based on signal feed through scheme is proposed. The basic ideology behind these FF designs is that all FF work as a D-FF (data-FF) but with different techniques so as to enhance the performance of the design. . From all these FFs, pulse triggered based FFs are mostly preferred due to their single latch structure and better power efficiency. The possible reduction in the power consumption of the proposed design incorporates for the power budget and many other benefits.

II. EXPERIMENTAL DETAILS:

2.1 Existing Design System:

Modified hybrid latch FF is the design comprising with less number of transistors, because it is having a semi latch structure. The pre charging of the node is completely dependent on the output and the data signals. There are many design comprising of FF but each design differ in their structure or techniques in order to optimize area, power, and delay. In order to keep the node x at logic '1' weak pullup transistor P1 is used for this purpose. This design has got a longer delay and average power consumption which is further minimized to a greater extent in the proposed system. The N2 and N3 transistors provides a better discharging operations. This design association with node x which becomes a floating point if data Q output are logic high.

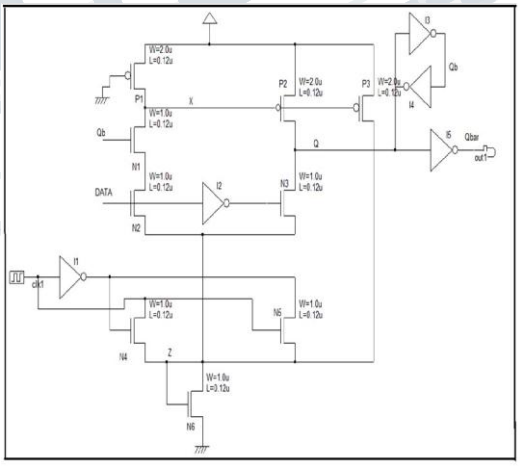

Fig 1: schematic of modified hybrid latch FF

2.2 Proposed FF Design:

In proposed design system the dual signals are regulated by the transmission gates that is clocking and data signals in order to optimize power factor, at an instance when there will be no switching. It results in low leakage power. A separate clock pulse generator circuit have been implemented which generates clock pulses when the clock transits from low to high. TSPC (True single phase clock) and transmission gates are combined in this proposed structure which lead to a faster D-FF. At

low clock pulse, transmission gate will be OFF that makes node z as 0. When clock pulse is high transmission gate will be ON node z will not be zero but due to some delay by the inverters in this case node z will be 0. The proposed design uses signal feed through technique by transistor N4 which is also connected to input data, this leads to a faster operation. Whatever may be the input data with the cock pulse generation N4 becomes ON which discharges the output Q very rapidly. Hence the proposed design is very much efficient in providing faster discharging operation, low leakage power and low average power dissipation.

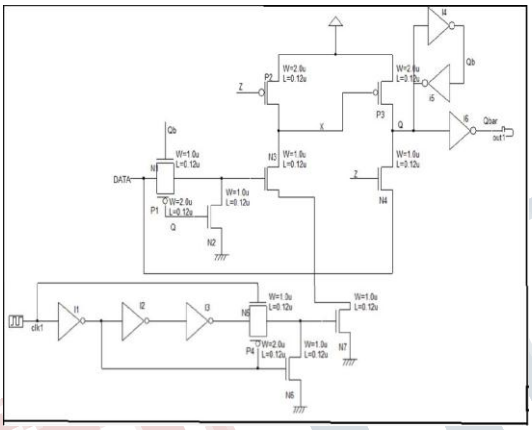

Fig 2: proposed conditional pulse control TG- FF

III. SIMULATION RESULTS:

The performance of the proposed design against the previous design is evaluated by using simulation. The following simulation results are implemented on H-SPICE tool which shows the average power and the delay minimization. The width of the clock pulse is a crucial part in operation hence a set up model is designed

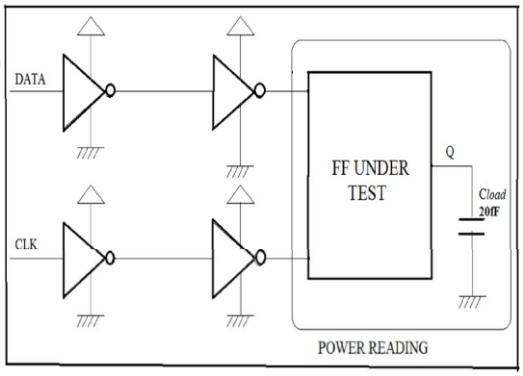

Fig 3: Simulation set up model

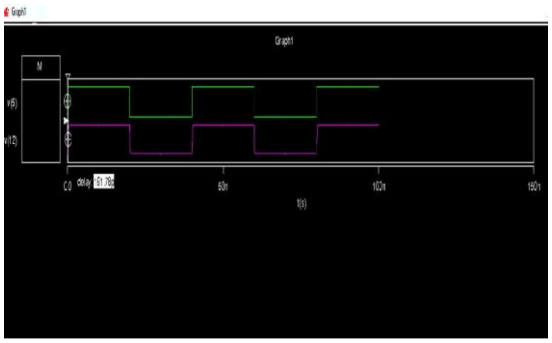

Fig 4(a): Simulation results showing Delay in previous design system (MHLFF)

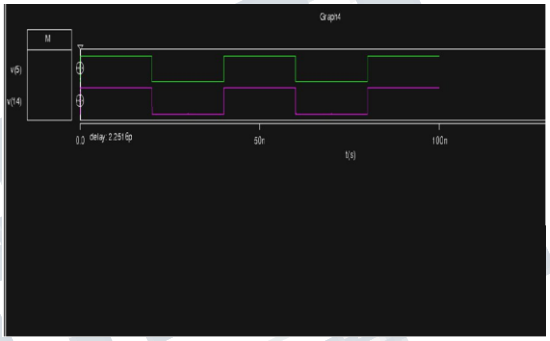

Fig 5(a): Simulation results depicting delay in the proposed design (CPCTG) FF

```
******
*extension pdff
******  transient analysis              tnom=  25.000 temp=  25.000
******
  avg_power=  1.0294E-05  from=  0.0000E+00     to=  1.0000E-07

          ***** job concluded
****** HSPICE -- A-2008.03 32-BIT (Feb 26 2008) winnt ******
******
*extension pdff
******  job statistics summary          tnom=  25.000 temp=  25.000
******

        total memory used        308 kbytes

# nodes =      17 # elements=      26
# diodes=       0 # bjts    =       0 # jfets   =       0 # mosfets =      23
# va device -    0

  analysis          time    # points   tot. iter  conv.iter

  op point          0.02           1          14
  transient         0.42         101        1260         385 rev=       14
  readin            0.02
  errchk            0.03
  setup             0.02
  output            0.00
        total cpu time          0.59 seconds
        total elapsed time         1 seconds
            job started at  20:42:46 03/31/2016
            job ended   at  20:42:47 03/31/2016

Init: hspice initialization file: C:\synopsys\Hspice_A-2008.03\hspice.ini
```

Fig 5 (b): Average power in proposed design (CPCTG)

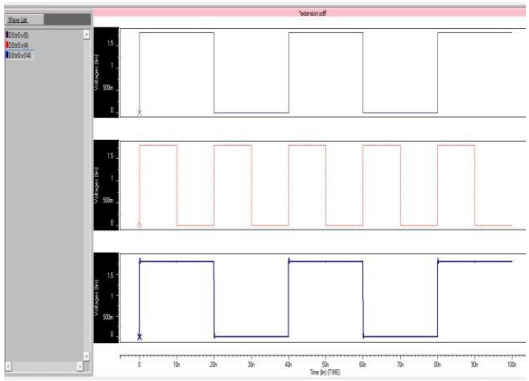

Fig 5(c): simulation results of CPCTG-FF

IV. CONCLUSION

A flip flop is designed which comprised of dual functionality incorporated with transmission gate which reduces power dissipation and employed with signal feed through scheme which faster the operation thereby reducing delay factor. The simulated results proof that the average power and delay is reduced compared to previous.

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