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Power Consumption Analysis of Homogeneous and Reconfigurable Router

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***Abstract*— Router is an essential component of Network-on-Chip(NoC). Conventionally used homogeneous router provide good throughput but buffer slots are fixed and cannot be reconfigured to the requirement. Here it consumes more power as not all the buffer slots are used. To overcome this drawback, reconfigurable router is designed where in the buffer slot size can be varied. That is buffer slots in each channel can be used by other channels. This utilizes the router resources efficiently there by reducing the power consumption when compared to homogeneous. The homogeneous router is designed with 16 buffer slots and reconfigurable router with 4 buffer slots which are simulated using Xilinx 14.7. Power is calculated using Xpower Analyzer where reconfigurable router is consuming 2.13mW less power compared to homogeneous router.**

***Index Terms*— Crossbar Switch, First in First out (FIFO), Homogeneous Router, Multiplexers , Network-on-Chip(NoC), Reconfigurable Router.**

I. INTRODUCTION

System on Chip consists of many IP blocks, buses and physical links. For data to be transferred between various IP cores it requires a high performance interconnection. The traditional bus based architecture has been replaced by NoC. In NoC, large scale networks are scaled down and applied to the embedded system-on-chip. NoCs consists of mainly 3 components-routers, links and network interface. Links physically connects the nodes and implement the communication. Router implements the communication protocol. Network interface makes the logic connection between the IP cores and the network. The basic requirements of the router design are performance requirement, low area and low power.

SOCS will have to provide a functionally-correct, reliable operation of the interacting components. The physical interconnections on chip will be a limiting factor for performance and energy consumption. Integrated solutions to challenging design problems in the communications among different IP cores are described in [1]. NoC is a new paradigm able to integrate a significant number of IP cores keeping high communication bandwidth. NoC considered here follows 2-D mesh network [2]. The heterogeneous integration of components in NoC architecture and modeling of reconfigurable components, IP cores is demonstrated in [3]. Implementation of dynamically reconfigurable NoC router with bus based interface is described in [4]. In an NoC several items can vary from design to design, like FIFO depth, router topology, switch, this is demonstrated in [5]. The router architecture in [6] has a fixed and large FIFO which can be dynamically reconfigured on requirement. Router architecture proposed by Matos[7] consists of 4 channels namely north, east, west and south. Channels are interconnected through the crossbar switch. Each channel consists of five multiplexers, two multiplexers are used to control the input and output of data, three multiplexers are used to control the read and write operation of FIFO. When the FIFOs of a channel are filled it can barrow more space from the right and left neighboring channel FIFO, if free slots are available in the neighboring channel. In the experiments conducted by [8] the FIFO buffers were the largest leakage power consumers, dissipating approximately 64% of the whole power budget. There by, FIFO buffers were considered for leakage power optimization. In homogeneous router architecture, there may be idle buffer slots which are not used and there by power and area consumption is high.

To overcome this, reconfigurable router architecture is designed in which buffers with smaller depth are used to perform the routing action same as homogeneous router with bigger buffer depths.

The principle in reconfigurable router architecture is that it can lend or borrow buffer slots to/from the neighboring channels. When a channel does not need its entire buffer slots, it can lend the slots to the neighboring

channels. When a channel needs more buffer slots than allocated and if free buffer slots are available in the neighboring channel it can borrow the buffer slots from the neighboring channel.

II. IMPLEMENTED WORK

A. *Implementation Of Homogeneous Router Architecture*

The router architecture consists of four channels, namely east, west, south and North Channel. These channels are connected through crossbar switch. Each channel consists of a FIFO and a multiplexer. South channel is shown in Fig 1.din is the input to the FIFO and dout is the output of multiplexer. As shown in Fig.1, each channel consists of a FIFO of size 16 and a 16:1 multiplexer. The size of the FIFO is defined at the design time and the size of FIFO is fixed and it can't be varied. As the size of FIFO buffer increases the size of multiplexer increases. There by the FIFO and multiplexer size varies linearly. The south channel design is replicated thrice to get the north, west and east channels. These channels are further connected using crossbar switch as shown in Fig.2. din_N,din_S,din_E and din_W are the output of crossbar switch.

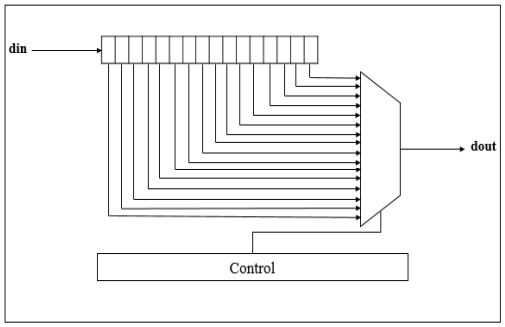

Fig.1 Homogeneous South Channel[7]

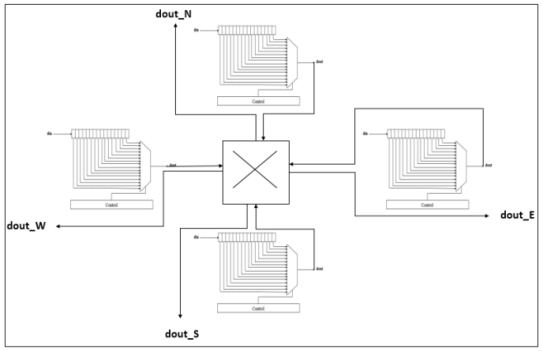

Fig.2 Homogeneous Router Architecture[7]

B. *Implementation Of Reconfigurable Router Architecture*

In reconfigurable router architecture each channel can have different buffer size. In this architecture it is possible to vary the buffer depths of each channel. Not all the buffer slots are used always. A channel can lend or borrow whole of its buffer slots or part of the buffer slots on requirement.

In this architecture each channel can use the buffer slots of the remaining three channels. By this way, each channel can have up to four times more buffer slots than the original buffer with the size defined at the design time. Fig.3 presents the south channel of the reconfigurable router. To allow the reconfiguration process each channel uses more multiplexers than the homogeneous channel. Each channel consists of six multiplexers, in which four are responsible for the reconfiguration process which controls the read and write process. Out of six, two multiplexers control the input and output of the data. As the depth of the buffer increases the size of the multiplexer also increases. When a channel fills all its FIFO buffer slots it can borrow the buffer slots from the neighboring channel.

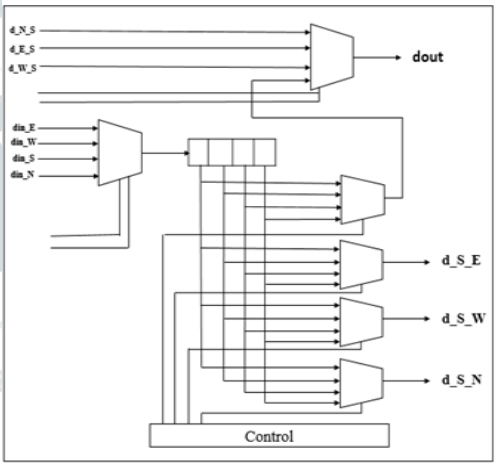

Fig.3 Reconfigurable South Channel[7]

As shown in Fig.3 each reconfigurable channel consists of six multiplexers and FIFO buffer. Each channel can receive four data inputs. For example let us consider south channel shown in Fig.3, having the following inputs: the channels own input din_S, input from right channel din_E, input from left channel din_W . For the purpose of illustration let us assume that the router we are using has a buffer depth equal to 4, and the router needs to be configured as follows: South Channel with buffer depth equal to 10, East Channel with buffer depth equal to 2, West Channel with buffer depth equal to 1, North Channel with buffer depth 3. In this case, South Channel needs to borrow 6 buffer slots from the neighbor. As the East Channel occupies two out of its four slots, this can lend two buffer slots to its neighbor. But still, South Channel needs four more buffer slots. West Channel occupies only one buffer slot, so it can lend three buffer slots to South Channel. North channel occupies three buffer slots and it

can lend one buffer slot to South Channel. There by, flits of the south channel are stored in East, West and North channel.

The flits stored must be sent to the output of South Channel. flits of South channel stored in East Channel are represented by d_E_S. Similarly d_W_S and d_N_S reperesnt flits of South Channel stored in West and North Channel. These flits are given as input to the multiplexer which controls the output.

South Channel consists the following outputs: its own output dout, and three more outputs d_S_E, d_S_W and d_S_N which are the flits of East, West and North Channel respectively stored in South Channel. dout is the output of the multiplexer which is the output of the channel.

Fig.4 shows the Reconfigurable Router Architecture in which the channels are connected using crossbar switch. dout_N,dout_S,dout_W and dout_E are the output of the crossbar switch.

III. RESULTS

Design implementation is done using Verilog and simulation is done using ISE simulator on XILINX 14.7 platform. Fig.5 and Fig.6 shows the output of all the channel and final output of crossbar switch of homogeneous and reconfigurable router respectively. All the channels are connected to the crossbar switch and final output is taken from crossbar switch.

Total power calculation is done using with the help of XPower Analyzer in Xilinx 14.7. Spartan 3 family is used for this purpose. Fig.7 and Fig.8 shows the total power dissipated by homogeneous and reconfigurable router.

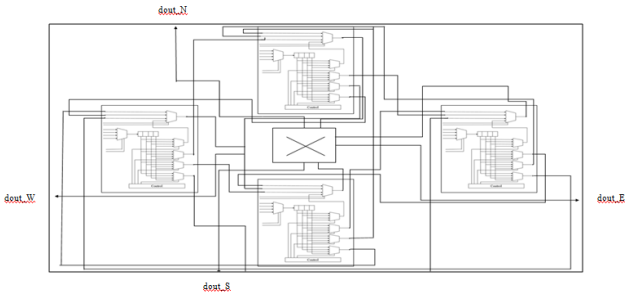

Fig.4 Reconfigurable Router Architecture[7]

From the Fig.7 and Fig.8 we can see that total power dissipated by homogeneous router is 62.38mW and total power dissipated by reconfigurable router is 60.24mW. There is a difference of 2.13mW, and there is a reduction in dynamic power.

Fig.5 Homogeneous Router Architecture

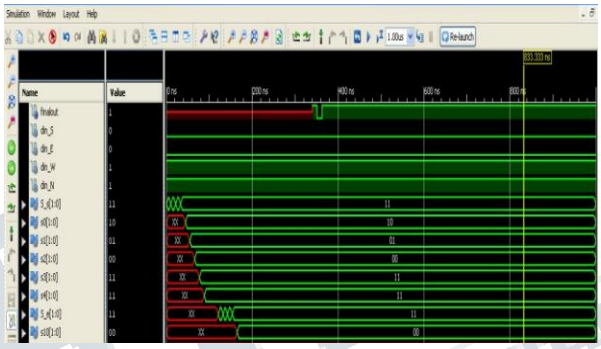

Fig.6 Reconfigurable Router Architecture

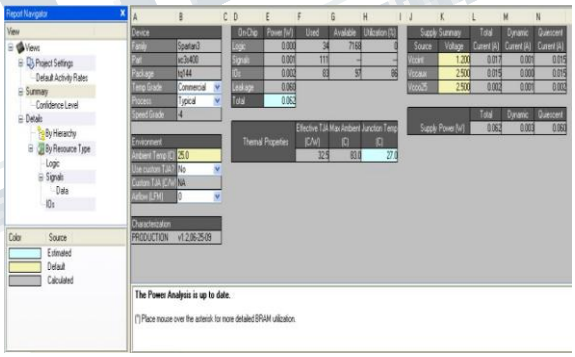

Fig.7 Total Power dissipated by Homogeneous Router

TABLE I
Power consumption of Homogeneous router

Power supply summary			
	Total	Dynamic	Static Power
Supply power (mW)	62.38	2.57	59.81

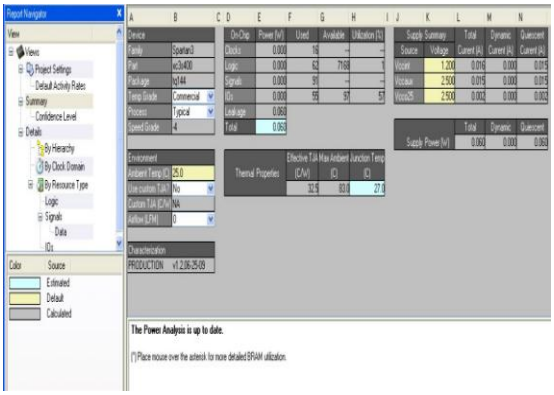

Fig.8 Total power dissipated by Reconfigurable router

TABLE II
Power consumption of Reconfigurable router

Power supply summary			
	Total	Dynamic	Static Power
Supply power (mW)	60.23	0.44	59.80

IV. CONCLUSION AND FUTURE SCOPE

Stack length of FIFO buffer is considered to be 16 for homogeneous and 4 for reconfigurable router. In reconfigurable router each channel can use the buffer slots of other three channel, there by each channel can have 4 times of its buffer slots. By this power consumption is less in reconfigurable compared to homogeneous.

But maximum combinational path delay for reconfigurable is 13.207ns and that for homogeneous is 12.190ns which is less compared to reconfigurable router.

With 16 slots in homogeneous and 4 in reconfigurable there is a power reduction of 2.13mW. Further there is a scope to design a reconfigurable router in which maximum combinational path delay can be reduced.

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