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SOC Design for IPTV Set Top Box

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Abstract: **IPTV is mainly used for Live Streaming, Time Shifting and provide Videos on Demand (VOD). In recent years of development in System on Chip (SOC) design the Ethernet transmission capability is 100Mbps.The data transmitted is in the form of packets through the Ethernet cable. This packet has to be converted into frames and stored in the memory. Generally, processor accesses the memory and stores the data in the form of frames in the memory. In the previous SOC design the Ethernet capability is 100Mbps and in this proposed design the Ethernet can provide up to 1Gbps transmission rate. HDMI used in proposed design. The quality of HDMI output is high compared with the previous VGA output. The signals enters through the Ethernet will be in encoded format so it has to be decoded using video decoder and it has to be processed to maximum quality of HDMI output (1080p).**

Keywords: **System on Chip, IPTV, HDMI, Set Top Box**.

I. INTRODUCTION

TV services have evolved from traditional linear TV to a plethora of new streaming services with the advent of IPTV. IPTVdiffers from traditional cable and other terrestrial technologies by delivering television program through different network technologies. IPTV provides some extra advantages such as ability to support VOD, ability to integrate TV program with some other IP based services, and the ability to response to customer's interactivity. IPTV services grouped into two types Live TV and VOD. Live TV uses IGMP to connect a multicast stream, while VOD uses RTSP to transmit media stream. For playback of TV program requires a either a PC or a STB

This work tries to describe aboutthe difference in picture clarity of VGA and HDMI. The aim is to design an iptv set top box with high speed data transmission rate if 1Gbps and to support low power HDMI 1.4 video display.

The remaining part of the paper is organized as follows. Section II describes the problem statement and related works. The proposed work is described in section III. The design and implementation details are found in section IV. Results and analysis are discussed in section V. Finally in section VI the conclusion and future work are stated.

II.STATE OF ART

A. IPTV

IPTV (IP Protocol TV)is an evolution of traditional TV to a advanced model TV based on digital network. In IPTV the content received through ethernet are shown in user display. The contents of IPTV are usually protected and users access the channel through STB which is connected to display [1]. In some cases, the users can use STB to access the channel which is connected to display. Other cases, the display and STB are integrated in a single device called SmartTV. IPTV is not similar to WebTV where users watch video over the Internet. There are some difference between WebTV and IPTV. For instance, WebTV is not limited to specific group of users as in case of IPTV. In WebTV the video streaming are send through internet but in case of IPTV the services are limited to particular group of users and it limited by geographic regions where the operator works [2]. WebTV does not care about the location from where the contents are served. In WebTV services usually the contents are not protected, users can able to visualize them without any restriction. In IPTV systems, the contents are usually protected from other users and it can be accessed through the STB connected to display. IPTV systems support bidirectional communication which allows receiving information from users. Therefore the SPs are able to manage the user access and provide necessary QoS.

B. STB

A set- top box is a device that connects television to broadband network for media processing. Traditional set-top box provides service only for television. But IPTV st-top box serves dual purpose of providing service for Television as well as Personal Computer. The main services are video on demand (VOD), electronic program guide (EPG), Personal Video Recording (PVR) and Linear TV. The other services oriented to PC devices are Web browsing, email, instant messaging (IM) and codec advanced multimedia [2]. The key elements for STBs are service provider and the requirements

of service provider defines prize and mechanism used to protect contents, software updates etc.

III. PROPOSED WORK

In this work, the IPTV set-top box is implemented in a SoC named Zynq 7020 of Xilinx. The SoC has two partitions namely the processing system and the programmable logic. The processing system has the ARM Cortex A9 processor and other hard IPs namely APU, USB, UART, SD card and Ethernet IPs. The programmable logic consists of configurable logic blocks, DSP slices and BRAMs.

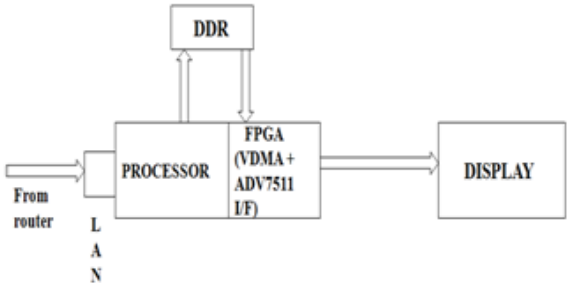

Fig1: Block diagram of IPTV

From Fig 1, it is observed that processor receives IP packets via ethernet and stores the received packets in DDR. Then the processor initiates the DMA engine. The VDMA engine starts reading the stored data in DDR and sends the HDMI interface.

A. Hardware Design of Proposed Work

The video frames are stored in SD card in binary file format. The size of this binary file depends on the number of frames and the frame resolution. In this work the resolution is 1080 pixels and the colour depth is 24 bits. Hence we derive the size of a single video frame as 1080*1920*24=6075KB. The maximum capacity of DDR is 512MB out of which 256MB is utilized for program memory and data memory. In the remaining 256MB approximately we can hold about (256*1024)/6075=43.15 frames. Using AXI writes the processor copies the video frame data from the SD card to the DDR memory. From DDR memory the DMA engine has to read the stored video frame data. The video frames are temporarily stored in the DDR in this manner in order to speed up the entire process. If the DMA engine tries to read directly from SD card, due to long inter-chip communication the data retrieval process become slow.

The VDMA engine reads the frame data from the DDR and holds it in a small buffer before transferring it to the HDMI display controller. The pixel clock for the display controller is 82.5MHz, but the processor clock is 660MHz. The processor is much faster compared to the display controller. Due to the high operating frequency of the processor it can meet the data requirement of the display controller and also monitor and control other peripherals like Ethernet, UART and SD card.

B. VDMA

The VDMA is video direct memory access. Whenever there is a requirement of high speed transfer of data for a peripheral outside the chip, direct memory access is preferred. Direct memory access is initiated by the processor[4]. Once initiated, the controls of the memory buses are taken over by the peripheral. Without any intervention by the processor, the peripheral starts the reading or writing the data. In this case direct memory access of DDR3 is done for providing high speed data transfer to the display control unit. Video DMA is a special kind of DMA IP, designed to support video applications. VDMA once programmed by the processor, continuously reads data from the DDR3 memory and transfer it to the display control unit. The size of the DMA buffer varies with the resolution of display. As the resolution increases, more data buffering is needed.

C. VDMA Hardware

S_AXI_LITE port is connected with M_AXI_LITE port of the processor and it configures the control registers of VDMA through this port.M_AXI_MM2S is connected to DDR and M_AXIS_MM2S is connected to HDMI hardware.

D. HDMI Hardware interface with VDMA

The HDMI hardware is packaged with slave AXI stream interface (S_AXI_MM2S) and the Master AXI_MM2S port of VDMA is connected to slave AXI _MM2S port of HDMI hardware[5]. VDMA receives the data from DDR through M_AXI_MM2S and HDMI hardware receives data from VDMA through M_AXIS_MM2S.

E. VDMA Configuration

The video frame buffer start address is written to the START_ADDRESS register. Then the horizontal size of the frame is written to the HSIZE register and the vertical size of the frame is written to the VSIZE register. The start bit VDMACR.RS is set to 1.All the registers have predefined offset from the base address defined in VDMA product guide and the register writes are carried out by the processor.

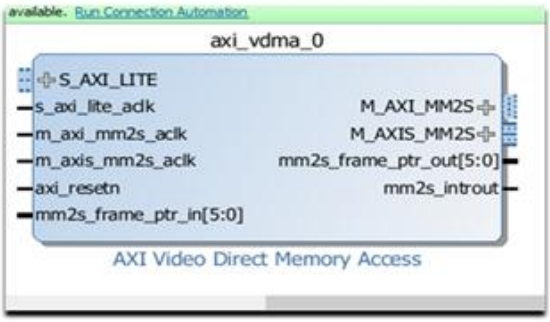

Fig 2: Motion Estimation Hardware Architecture

IV. IMPLEMENTATION

Once the hardware block is designed, bit stream can be generated using Vivado. All the hardware information is exported to Software Development Kit (SDK). The SDK holds the hardware information in hardware definition file. The hardware definition file has information such as device start and end addresses that are mapped to DDR memory.

The software that runs on top of the hardware can be a bare metal code or an operating system. In this case an operating system is preferred over the bare metal code. The bare metal code can have control only over a single core of the processor. But the operating systemhas a scheduler to overcome this bottleneck. The scheduler manages the load and distributes it over the processor cores.

The operating system chosen here is Xillybus operating system. This operating system is based on Linux. The basic functions such as network driver, DDR controller, SD card driver are available by default in the kernel. Since the HDMI display hardware is newly added, driver has to be developed separately and attached with the kernel later.

There are four basic files required to run the Xillybus operating system namely the kernel image, the device tree, first stage boot loader and second stage boot loader. The kernel image has the basic drivers to run the operating system. The device tree has the information to partition the RAM area into sections and each section is mapped to a hardware resource. The first stage boot loader loads the bit stream in the FPGA and gives the control to second stage boot loader. The second stage boot loader loads information such as network address, gateway address, net mask and physical address of the hardware and hands over the control to the kernel.

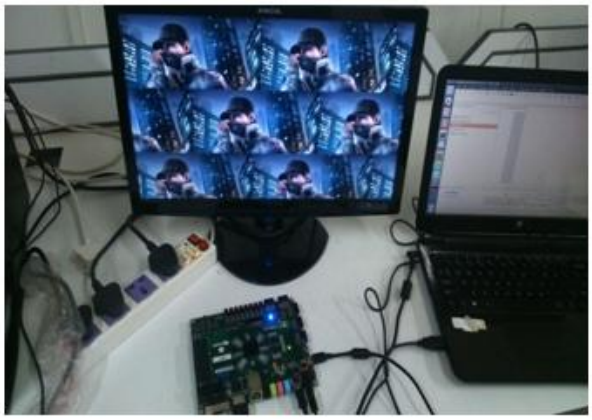

Fig 3: 480p image tiled in 1080p display

V. RESULTS AND ANALYSIS

The hardware and software implementations of IPTV set-top box are compared. There is variation in power consumption and hardware utilization.

A. Resource Utilization

In RTL view, the top module holds the vdma and reconfigurable adv7511 interface modules. From fig. The number of used cells is very less compared to the number of unused cells. The percentage of occupied slices is found to be 31 % of total number of available slices.

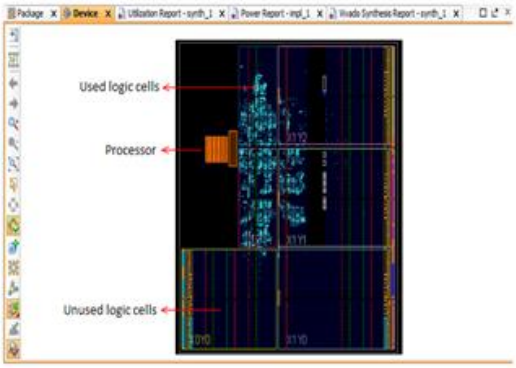

Fig 4: Resource utilization in FPGA

B. Power consumption

The main advantage of using FPGA based video display is power consumption. FPGA consumes very less power compared to processor based set-top boxes. From the Vivid power report, the power consumption is estimated to be 1.78 W.

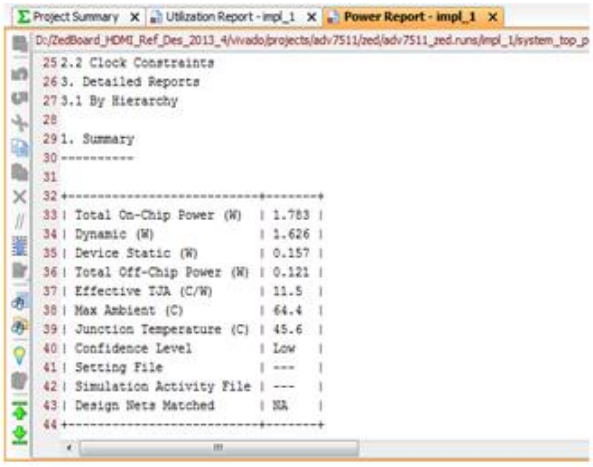

Fig 5: Power consumption

VI. CONCLUSION AND FUTURE WORK

In this work, video display controller is implemented in FPGA with 1080p resolution and HDMI support. Work done in ethernet controller and display controller is integrated to get a continuous stream of video data. Audio and Video signals are synchronized in order to carry out parallel video and audio reception for continuous streaming. In future, Codec can be implemented in order to process the compressed data.

REFERENCES

[1] Taeseok Kim and HyonKyungBahn, "Implementation of Storage Manager for an IPTV Set -Top Box" IEEE Transaction on Consumer Electronics, Vol.54, No.4, pp 1770-1775, November 2008.

[2] ShiguoLian and Zhongxuan Liu, "Secure Media Content Distribution Based on the Improved Set-top Box in IPTV" IEEE Transactions on Consumer Electronics, Vol. 54, No.2, pp 560-566,May 2008.

[3] Christopher A. Chambers, "Designing a Set-Top Box Operating System", IEEE, pp 368-369,1995.

[4] Ivan Bernabe Sanchez, Daniel Diaz-Sanchez, Mario Munoz Organero, "A Flexible Software Architecture for IPTV Set-top Boxes",IEEE Second International Conference on Consumer Electronics,2012.

[5] **ADV7511** Low-Power HDMI 1.4 Compatible Transmitter with Audio Return Channel Programming Guide.

[6] **AXI VDMA** v6.2 LogiCORE IP Product Guide.

[7] AbdelrahmanAbdelazima, Martin Varleya and DjamelAit-Boudaoudb, "Effect Of The Hadamard Transform On Motion Estimation Of Different Layers In Video Coding", International Archives of Photogrammetry, Remote Sensing and Spatial Information Sciences, Vol. 38, Part 5 Commission V Symposium, Newcastle upon Tyne, UK. 2010

[8] Armando Mora Campos , Francisco J. BallesterMerelo, Marcos A. Martı´nezPeiro, Jose A. Canals Esteve, "Integer-pixel motion estimation H.264/AVC accelerator architecture with optimal memory management", journal on Microprocessors and Microsystems vol. 32 pp. 68–78.