

Self - Repairing SRAM using Closed-loop Adaptive Compensation Algorithm

^[1] Spoorthi Y ^[2] Nalina H D ^[3] Thilgavathy R
^{[1][2][3]} Assistant Professor, Department of ECE,

GSSS Institute of Engineering & Technology for Women [GSSSIETW], Mysuru, India

Abstract: In nanometer scale static-RAM (SRAM) arrays, systematic inter-die and random within-die variations in process parameters can cause significant parametric failures, severely degrading parametric yield. In this paper, we investigate the interaction between the inter-die and intra-die variations on SRAM read and write failures. To improve the robustness of the SRAM cell, we propose closed-loop adaptive compensation algorithms that directly sense the global read stability and writ ability of the cell. The main aim of the of the proposed scheme is to design a sensor that directly sense the global read stability and writ ability of an SRAM die and apply proper cell correction/compensation mechanism using cell and peripheral supply voltages to mitigate the dominant type of failure. Since the direct sensing of the global read stability and write-ability helps to successfully distinguish global corners of nMOS and pMOS devices, the proposed scheme becomes more effective in reducing the parametric failures.

Keywords— SRAM (Static Random Access Memory), RBL (Read Bit Line), RWL (Read Word Line), WWL (Write Word Line), VTN (Threshold voltage), VSAT (Saturation voltage)

I. INTRODUCTION

Due to the high density requirement for embedded memories, such memories are highly vulnerable to process variation induced failures. A conservative design approach can largely affect memory density and access performance. This project analyzes variation effects in SRAM and presents low-cost, adaptive post-silicon repair mechanisms. In this paper, we propose a scheme for post-silicon adaptive repair of SRAM array considering the strong relationship that exists between systematic inter-die variations and random within-die variations. The novelty of the of the proposed scheme is to directly sense the global read stability and write-ability of an SRAM die and apply proper cell correction/compensation mechanism using cell and peripheral supply voltages to mitigate the dominant type of failure. Since the direct sensing of the global read stability and write-ability helps to successfully distinguish global corners of nMOS and pMOS devices, the proposed scheme becomes more effective in reducing the parametric failures. It is possible to apply the proposed scheme by applying full functional test to memory array multiple times. First to detect whether the number of read or write failures, next, to ensure that the adaptive repair scheme did not introduce any new failures and taking appropriate decisions, and finally, before shipping the products. The proposed SRAM array with adaptive repair algorithm has an improved parametric yield compared to the SRAM array with no adaptive repair mechanism.

The following are the salient scope of the proposed compensation adaptive technique.

- a) Direct detection of the global Read and Write corners.
- b) Consideration of the pMOS and nMOS V_t 's as separate process parameters.
- c) Cell corrections can be applied through the proper choice of voltage signals (V_{DD} and/or V_{CS})—suitable for PD/SOI as well.
- d) No dynamic change in signals-simple design and timing.
- e) Iterative closed loop compensation scheme improves the parametric process yield significantly.

II. THEORY BACKGROUND: JOINT IMPACT OF INTER-DIE AND INTRA-DIE SHIFT ON SRAM STABILITY

The systematic (or global) variation equally modifies the characteristics of all the NMOS and PMOS devices in an SRAM die. However, the global variation in NMOS AND PMOS devices can be different from each other. On the other hand, local random variation results in mismatch between neighboring devices in a die. This is illustrated in Figure.2.1 for threshold voltage (V_T) variation in a process.

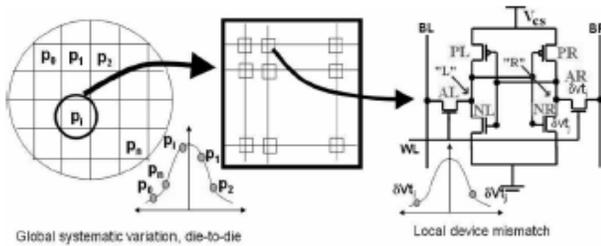


Figure 2.1: Global systematic and local random variation in device threshold voltage degrades yield of SRAM design.

First, the V_t of all nMOS (and pMOS) devices in a die is shifted from its designed value by a certain amount due to global systematic variation. Next, if a single die is considered, the V_t of different devices in an SRAM cell in that die can vary from its global value due to local random variation. The local random variation results in mismatch between different devices in the cell and is the primary cause of parametric (read and write) failures in SRAM [3]. The global variation modifies the V_t of all the nMOS devices in the cell by same amount and all the pMOS devices by same amount. However, the global shift in nMOS and pMOS devices can be different. To illustrate the interaction of the global inter-die and local random V_t variations on SRAM stability, we consider SRAM write failure. The write failure occurs if the node storing “1” in an SRAM cell cannot be discharged to “0” during the wordline “ON” time. The write failure becomes more probable if the discharge current through the access transistor in an SRAM cell (Figure.2.1) reduces.

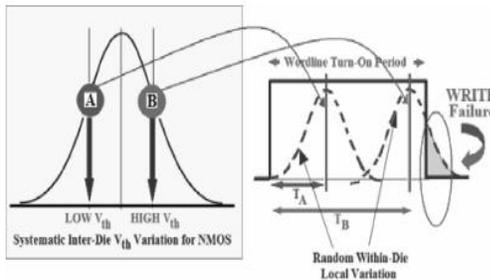


Figure 2.2: Inter-die V_t variation pushes the cell towards the failure point but within-die variation causes the actual failure.

Consider two SRAM dies from two different global corners and assume that the local variations in both dies are the same. Further, consider die “A” from a low and die “B” from a high nMOS global corner. Write failure in an SRAM cell is a strong function of the strength of access transistors (AL, AR in Fig. 2.1) [6].

Assume that the time required discharging the node “L” from logic “1” to logic “0” for two different

dies “A” and “B” be T_A and T_B , respectively. The global variation shifts the nominal value of the write time and due to higher V_t of nMOS, $T_B > T_A$. The local variation results in a variation in the write time for different cells in the array.

Hence, for the same amount of local variation, SRAM array which has a higher nominal write time is expected to have a larger number of cells with faulty write operation as illustrated in Figure. 2.2. Thus, the total number of faulty cells in an SRAM array is not only a function of the local within-die variation, but, also a strong function of the global inter-die variation.

III. PROPOSED ARCHITECTURE

The below Figure 3.1 illustrates the overall system architecture of the proposed SRAM array with adaptive repair mechanism. It includes the conventional SRAM array with on-chip circuits for failure characterization, a global read stability and write-ability detector, a very simple digital logic circuit for making decision on whether read or write correction is required, and a circuit for generating the adaptation signals for the required cell corrections.

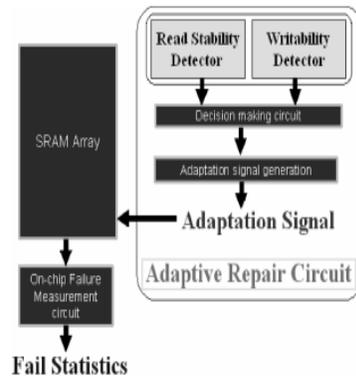


Figure 3.1: System diagram of the self-repairing SRAM array with on chip monitor and compensation circuitry

The read stability and write-ability detectors detect the global read and write stabilities. They detect whether a read or a write correction is required, and accordingly generate proper digital signals (“0” or “1”) to actuate the “Decision making and Adaptation signal generation” block that applies a proper voltage (V_{HIGH} or V_{LOW}) to the word line (V_{WL}) and cell supply terminal(V_{CS}).

After the proper type of correction has been done, the read and write stabilities of the array with modified cell terminal voltages are re-detected to avoid any overcorrection’s that might degrade the process yield. This second level of stability detection ensures the fact that an array corrected for read stability does not fail in terms of write-ability and vice versa. If the second level of stability detection shows that both the read stability and write-

ability are above the correction boundaries, the array is placed in the “CORRECT ARRAY” bin, otherwise it is placed in the bin tagged as “Array Suffering from Stability.” A regular functional test of the memory array is performed for all the dies in “CORRECT” and “Suffering from Stability” bins before shipping.

Interestingly, it is possible to apply the proposed scheme by applying full functional test to memory array multiple times. First to detect whether the number of read or write failures, next, to ensure that the adaptive repair scheme did not introduce any new failures and taking appropriate decisions, and finally, before shipping the products. It should be noted that the proposed read stability and write-ability detection scheme does not replace the regular functional tests; it only helps in correction of parametric read/write failures.

IV .DESIGN PRINCIPLES & ANALYSIS OF INDIVIDUAL SYSTEM COMPONENTS

In this section, we focus on the design issues associated with three major components of the self-repairing SRAM array and evaluate their effectiveness to the overall system yield improvement. As depicted in Figure 4.1, the read stability detector, write-ability detector and the correction scheme using proper word line and cell supply voltages constitute the heart of the system and accordingly, the overall system performance highly depends upon the efficient design of these individual building blocks.

A: Design of the Read Stability Detector

The major challenges in designing the read stability detector is the identification of a metric that accurately capture the global read corner of the memory array. To capture the cell read stability, we propose a monitor to sense the difference between trip voltage (V_{trip}) of the half-cell composed of PL, AL, NL, and read disturb voltage (V_{read}) of the half-cell composed of PR, NR, and AR (Figure 4.1).

To measure the trip voltage, the input and output of the inverter PL-NL are connected; the AL device has gate at V_{WL} and drain at V_{CS} , the feedback path connecting nodes “L” and “R” is eliminated, and the voltage at node “L” is measured.

To measure the read distributed voltage, gates of PR and NR are connected to V_{CS} , gate of AR is at V_{WL} , drain of AR is at V_{CS} , the feedback connection for nodes “R” and “L” is removed, and the voltage at node “R” is measured.

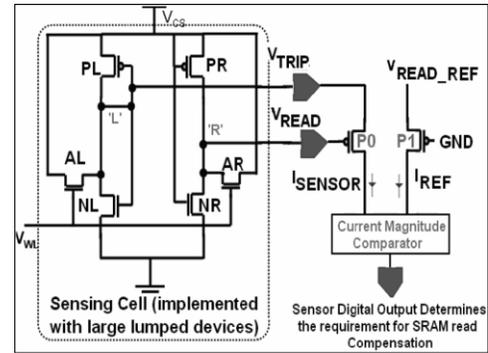


Figure 4.1: SRAM global read stability sensor ($V_{trip}-V_{read}$)

Next, V_{trip} and V_{read} are connected to the drain and gate of pMOS (P0) of a differential pMOS pair, respectively. The other pMOS (P1) of the pair has gate at GND and drain at V_{ref} .

The current through the two pMOSs are compared using a current comparator [2]. The differential pair needs to be properly matched. If the ($V_{trip} - V_{read}$) falls below a certain level (V_{READ_REF} in Figure 3.3) which corresponds to a minimum tolerable value of normalized read stability, then current through the reference pMOS (P1) becomes larger than that through the sensing pMOS (P0), and the output of the current comparator indicates that read correction is required (Figure 4.1).

The SRAM cell used for sensing read/trip voltages needs to be designed with large devices to minimize the effect of local variations on those voltages. This can also be achieved by properly configuring and connecting a large number of actual SRAM cells in parallel.

B Design of Write-ability Detector

For write-ability sensor, the SRAM cell designed with large devices (or by connecting cells in parallel), is used to capture the feedback effect which plays an important role in write operation (Figure 4.2).

First, when the word line signal is low, node “L” is pre-charged to “1” and node “R” is pre-discharged to “0.” The bitline R is held at V_{DD} whereas a V_{WRITE_REF} (>0) is applied at the bitline “L.”

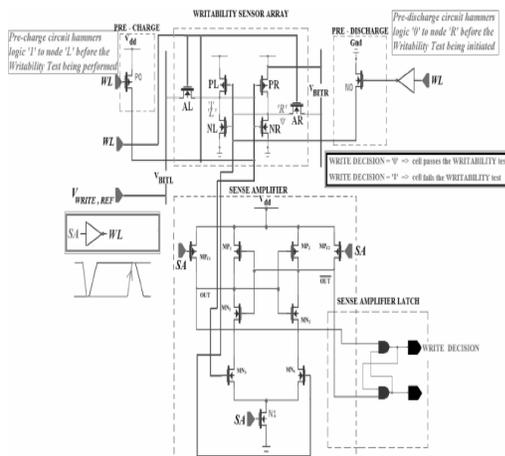


Figure 4.2: SRAM global write-ability sensor.

When the WL signal goes high for write operation, node “L” discharges to “0” whereas node “R” is charged to “1.” Voltages at both nodes are sampled at the negative edge of the word line signal and compared. If node “L” voltage is less than node “R” voltage at that time, the comparator indicates that the write operation is correct. If a correct write operation can be performed at a higher value of V_{WRITE_REF} , it indicates that the write-ability (write margin) of the cell is high.

Hence, for global corners with good write-ability (i.e., less prone to write failures), the cell will be able to perform a correct write operation even with a high value of V_{WRITE_REF} .

During measurement, V_{WRITE_REF} value is applied to all the SRAM dies. For SRAM arrays where proper write operation cannot be achieved with this reference value of V_{WRITE_REF} , the sensor should indicate that a write correction is required.

Note that, since the sensor operates using transient WL signal, it also captures the frequency dependence of write failures. As in case of “global read stability detector,” in this case the devices in the sensor cell either need to be large or need to be designed by connecting a large number of actual cells in parallel to minimize the impact of local random variability.

In order to sense the cell write-ability, we store a “0” at node “R” and “1” at node “L.” This time we have “ V_{DD} ” connected to the bitline “R” and a variable voltage on the bitline “L.” As soon as the word line turns on, node “R” tries to get charged to “1” and node “L” tend to discharge to “0.” The tendency of node “L” to discharge to zero is a strong function of the variable voltage. Lower the value of V_{WRITE} (it can vary only between 0 and V_{DD}),

worse is the cell write-ability. The variable voltage is defined as “weak write test output”. In our proposed scheme, we sense the SRAM cell write-ability as described as follows.

- a) First, we determine the voltage V_{WRITE} required to flip the cell under nominal V_t conditions.
- b) Apply the voltage as predicted above to the port “ V_{WRITE_REF} ” in Figure 4.2
- c) If the cell flips, we conclude that no write correction is required (i.e., the cell is already in a good write corner), but if it does not, write correction is applied.

V.RESULTS

The simulation results of SRAM Read and Write operation, SRAM read good, read faulty, and read compensation, SRAM write good, write faulty, and write compensation waveforms are generated using Synopsys H-SPICE

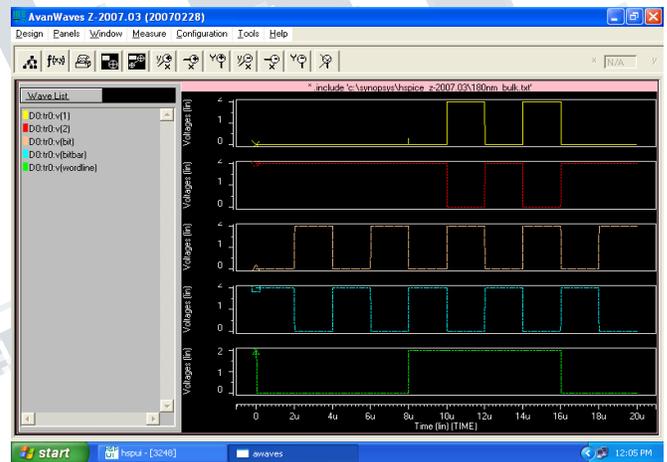


Figure 5.1: H-SPICE -SRAM write operation

The write operation begins, when the word line is from 0-1 transition, whatever the content stored in the bit and the bit bar will be transferred to node (V1 & V2) respectively(Figure 5.1)

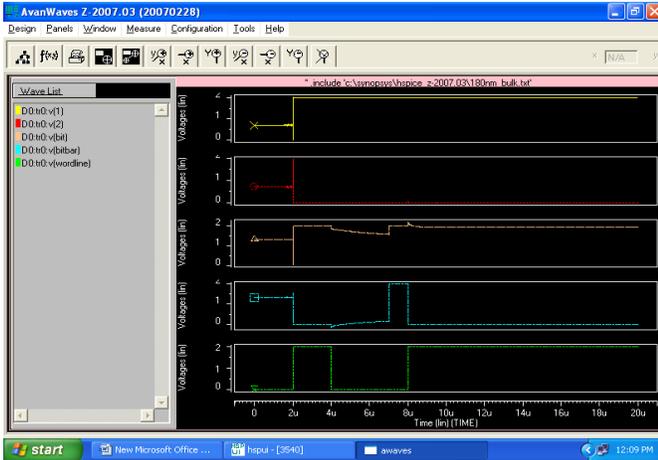


Figure 5.2: H-SPICE- SRAM read operation

Read cycle is started by pre-charging both bit & bitbar to 1, then asserting wordline. Values stored at node (V1 & V2) are transferred to the bit lines by leaving bit at its pre-charged value and discharging bitbar to 0. (Figure 5.2)

Here, $I_{\text{sensor}}(i_7) = 22.11\text{nA}$, $I_{\text{ref}}(i_8) = 10.86\text{nA}$, $V_{\text{thn}} = 0.4\text{V}$, $V_{\text{thp}} = -0.42\text{V}$, $V_{\text{wl}} = 1\text{V}$. Since, $I_{\text{sensor}}(i_7) > I_{\text{ref}}(i_8)$ the read operation is good, hence there is no need of compensation. (Figure 5.3)

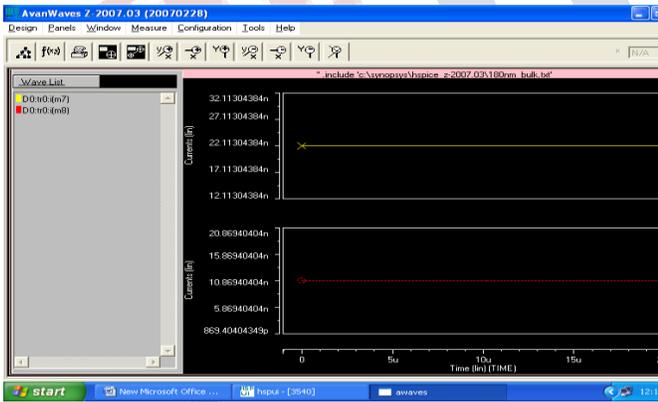


Figure 5.3: H-SPICE- SRAM good read operation

Assuming, due to fabrication fault the threshold voltage of V_{thn} and V_{thp} has changed. So the read stability detector detects that $I_{\text{sensor}}(i_7) < I_{\text{ref}}(i_8)$, hence there occur a faulty read operation. Hence it requires a read compensation.

Here, $I_{\text{sensor}}(i_7) = 7.819\text{nA}$ & $I_{\text{ref}}(i_8) = 10.86\text{nA}$, $V_{\text{thn}} = 0.32\text{V}$, $V_{\text{thp}} = -0.34\text{V}$, $V_{\text{wl}} = 1\text{V}$ (Figure 5.4)

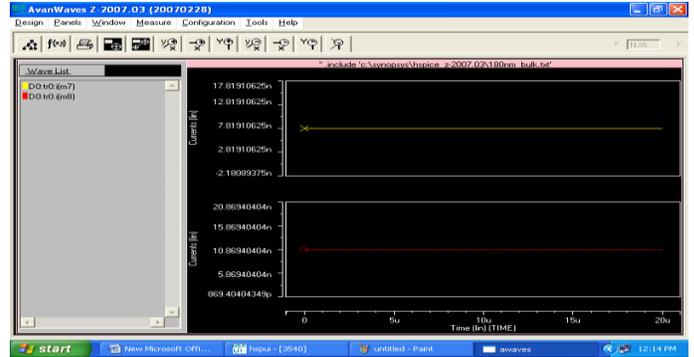


Figure 5.4: H-SPICE -SRAM faulty read operation

Assuming, due to fabrication fault the threshold voltage of V_{thn} and V_{thp} has changed, hence there occur a faulty read operation, by applying read compensation technique i.e changing $V_{\text{wl}} = 0.9\text{V}$, after changing V_{wl} Voltage, $I_{\text{sensor}}(i_7) > I_{\text{ref}}(i_8)$, it indicates that the read operation is good. Here, $I_{\text{sensor}}(i_7) = 17.75\text{nA}$, $I_{\text{ref}}(i_8) = 10.86\text{nA}$, $V_{\text{thn}} = 0.32\text{V}$, $V_{\text{thp}} = -0.34\text{V}$, $V_{\text{wl}} = 0.9\text{V}$ (Figure 5.5)

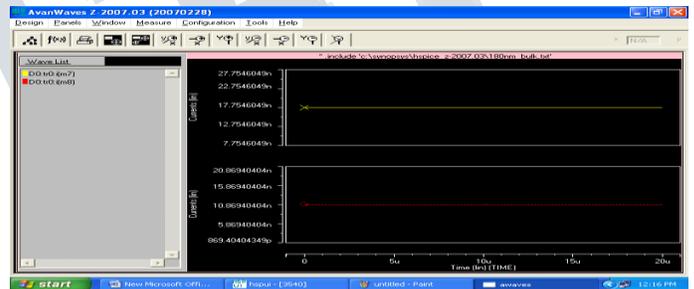


Figure 5.5: H-SPICE -SRAM compensated read operation

When the word line is from 0-1 transition, the data stored at bit and bitbar must be flipped to node (V1 & V2) respectively. Hence from the above graph it can be concluded that it is a good write operation. Here, $V_{\text{thn}} = 0.4\text{V}$, $V_{\text{thp}} = -0.42\text{V}$, $V_{\text{DD}} = 1\text{V}$. (Figure 5.6)

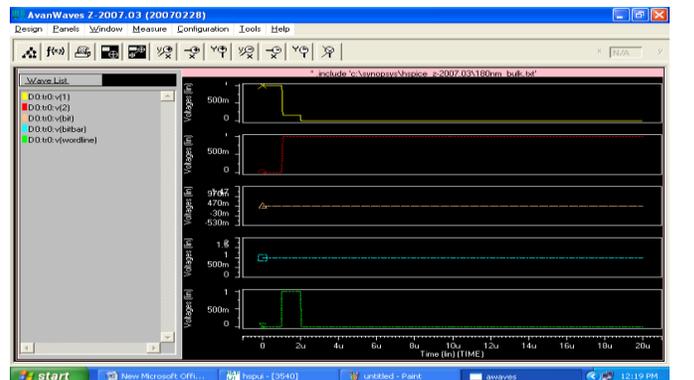


Figure 5.6: H-SPICE -SRAM good write operation

Assuming, due to fabrication fault the threshold voltage of V_{thn} and V_{thp} has changed.

So the write stability detector detects that there is error in flipping the data, i.e., the contents of bit & bitbar are not flipped correctly to node (V1 & V2) when wordline is from 0-1 transition, hence there occur faulty write operation. Hence it requires write compensation.

Here, $V_{thn}=0.32V$, $V_{thp}= -0.34V$, $V_{DD}=1V$.(Figure 5.7)

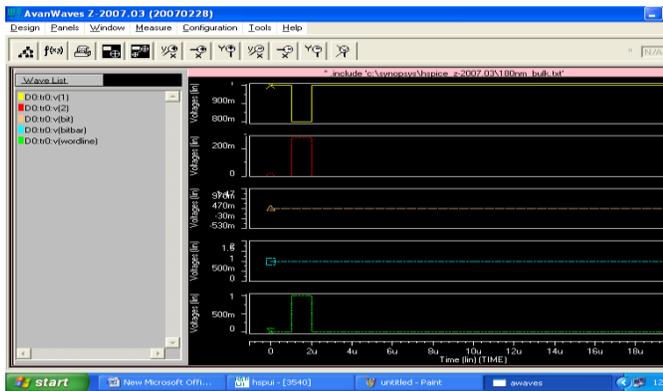


Figure 5.7: H-SPICE -SRAM faulty write operation

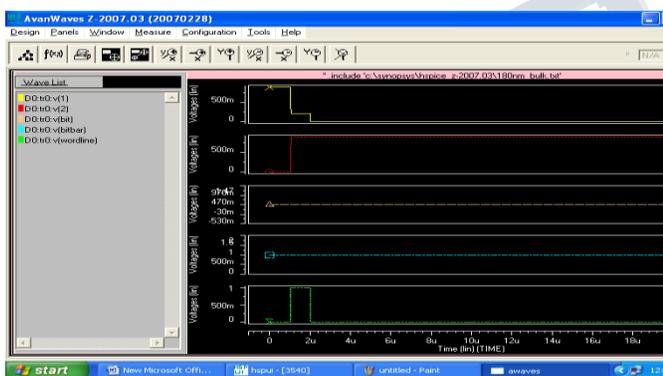


Figure 5.8: H-SPICE -SRAM compensated write operation

Assuming, due to fabrication fault the threshold voltage of V_{thn} and V_{thp} has changed, hence there occur a faulty write operation, by applying write compensation technique i.e changing $V_{DD}=0.9V$, after changing V_{DD} Voltage, the data stored at bit & bitbar are flipped correctly to node (V1 & V2) when the wordline is from 0-1 transition, indicating that write operation is good.

Here, $V_{thn}=0.32V$, $V_{thp}= -0.34V$, $V_{DD}=0.9V$.(Figure 5.8)

IV. DEVICE UTILIZATION SUMMARY OF READ AND WRITE OPERATION

Table 5.9: Device utilization summary

Number of Slices	4 out of 704 0%
Number of 4 input LUTs	8 out of 1408 0%
Number of IOs	13
Number of bonded IOBs	11 out of 108 10%

E. Speed Grade

Table 5.10: Speed Grade

Maximum combinational path delay	7.337ns (6.017ns logic, 1.320ns route) (82.0% logic, 18.0% route)
Total number of paths / destination ports	21 / 8

REFERENCES

- [1] A. J. Bhavnagarwala, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 658–665, Apr. 2001.
- [2] S. Jae-Yoon, Y. Hongil, C. Ki-Chul, L. Hyun-Seok, H. Sang-Pyo, L. Kyu-Chan, Y. Jei-Hwan, S. Dong-II, and C. Soo-In, "A 1.8-V 128-Mb mobile DRAM with double boosting pump, hybrid current sense amplifier, and dual-referenced adjustment scheme for temperature sensor,"
- [3] S. Mukhopadhyay, "Design of a process variation tolerant self-repairing SRAM for yield enhancement in nanoscaled CMOS," in Proc. IEEE Int. Test Conf., Nov. 2005, pp. 1126–1135.
- [4] S. Mukhopadhyay, "Reduction of parametric failures in sub-100-nm SRAM array using body bias," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 1, pp. 174–183, Jan. 2008
- [5] Niladri Narayan Mojumder, "A post silicon-tuning technique to improve parametric yield of SRAM array using body bias (BB)". in Proc. IEEE Int. Test Conf., Nov. 2009.
- [6] Z. GUO, S. BALASUBRAMANIAN, R. ZLATANOVICI, T.-J. KING, AND B. NIKOLIC, "FINFET-BASED SRAM DESIGN," IN PROC. LOW POWER ELECTRON. DESIGN, INT. SYMP., AUG. 2005, PP. 2–7.