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Low Noise Amplifier for the MICS band in CMOS 180nm Technology

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Abstract: **The main focus of this paper is to design a Low Noise Amplifier for the Medical Implant Communication Services (MICS) band. Low Noise Amplifier (LNA) is designed by utilizing the techniques of current-reuse, feedback and back gate coupling. Both nMOS and pMOS transistors are used to save power consumption and to enhance gain, common gate (CG) and Shunt feedback (SFB) topologies are combined. LNA achieves 10dB of Gain, 11.6dB Noise figure and -18dBm of IIP3. Simulations are done using H-SPICE in CMOS 180nm PTM Technology.**

Index Terms— Gain, IIP3, Low Noise Amplifier, Medical Implant Communication services (MICS), Noise figure.

I. INTRODUCTION

In 1999, FCC allocated spectrum band 402-405MHz for MICS applications. It allows bi-directional radio communication with electronic implants. The maximum used bandwidth is 300 kHz and gives a range of 2m distance. Basic requirements for MICS applications is to consume low power, device should have small size and to achieve data rate of minimum 200kbps. MICS specifies a maximum of -16dBm [effective isotropic radiated power (EIRP)] transmit power by base station so that it avoids interference with other communication services. This paper focuses on designing Low Noise Amplifier that can effectively improve Gain, Noise Figure and IIP3 for the MICS band.

II. LOW NOISE AMPLIFIER

In an RF receiver, input signal from an antenna first passes through the LNA that amplifies the signal and suppresses noise contributions from subsequent stages. Hence low noise figure and high gain are critical LNA performance parameters in portable applications. Namjun Cho, proposed a Dual-Band LNA that operates in 30-70Hz body channel communication (BCC) and 402-405Hz medical implant communication service (MICS) [1]. To support concurrent operation LNA is designed using cascaded LC tanks, which generates series resonance that is beneficial to suppress possible interferences at receiver. Power is shared and hence operating power can be saved. Stanley B.T. Wang, proposed fully differential CMOS LNA that operates below 960MHz [2]. They have used both nMOS and pMOS to reduce power consumption. To increase gin they have proposed Shunt feedback common gate hybrid LNA that combines shunt feedback amplifier and common gate amplifier. In [3], LNA is designed using inductor with bond wire that saves the chip area. The active balun generates noise, this noise can be suppressed by high gain LNA. This LNA achieves a gain of 27dB.Tino Copani, presents a low power CMOS LNA for medical implant applications [4]. A gm-boosted common gate differential LNA is implemented, cross coupling capacitors increases the gain of common gate devices. Noise impact of band pass filter is minimized by the gain provided by gm-boosted LNA.

In this paper, both nMOS and pMOS transistors are used so that current is reused and save power consumption which also boost the transconductance. To enhance the gain SFB and CG amplifier is combined to shunt-feedback/common-gate hybrid (SFBCG) topology. Resistors and transistors are used as passive and active feedbacks to reduce the input and output impedance.

III. LNA ARCHITECTURE ANALYSIS

A. Shunt-Feedback/Common-Gate (SFBCG) Hybrid LNA

1. Traditional wideband amplifiers

Resistor-terminated common-source amplifier, shunt-feedback amplifier and common gate amplifier are the most popular amplifiers used to provide both power/voltage gain and 50 Ω input impedance over a wide bandwidth (Fig.1). Most of the wideband LNAs are published based on either of these topologies. For example considering SFB amplifier, voltage gain of differential shunt-feedback amplifier is

$$A_V = g_m R_f - 1 \qquad (1)$$

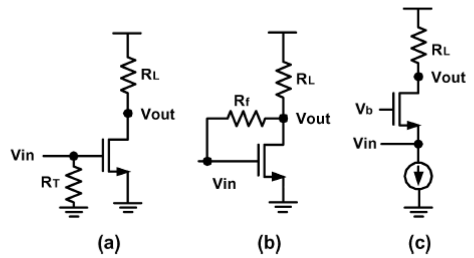

Fig.1 (a) Resistor-terminated common-source amplifier. (b) Shunt-feedback amplifier. (c) Common-gate amplifier

2. Adopting current-reuse technique

To reduce power consumption both nMOS and pMOS transistors are stacked together [7]. Transconductance changes from g_{mn} to $g_{mn} + g_{mp}$, for the same input resistance and noise figure the current is halved. Thus current-reuse technique is applied for shunt-feedback amplifier as shown in Fig.2(a) and for common gate amplifier as shown in Fig.2(b)

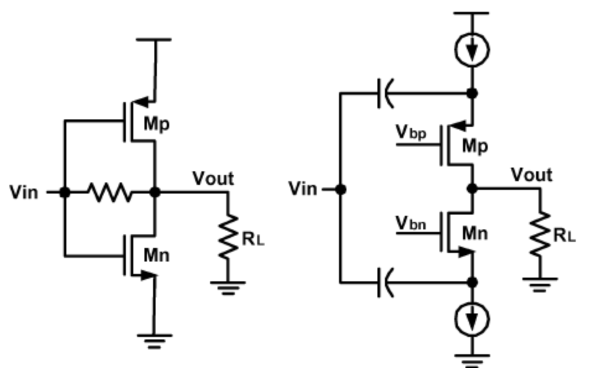

Fig.2 (a) shunt-feedback amplifier and (b) common-gate amplifier

SFBCG topology analysis

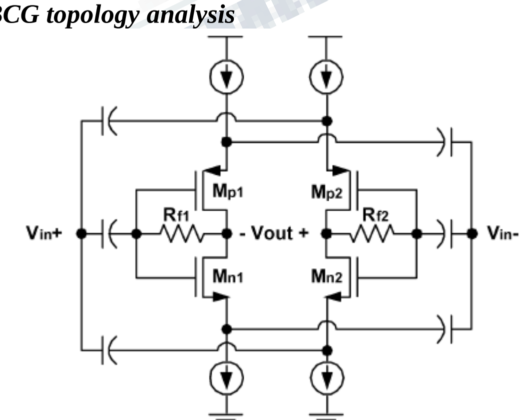

Fig.3 Shunt-Feedback/Common-Gate hybrid (SFBCG) amplifier

Shunt-feedback/common gate Hybrid topology is shown in Fig.3. In the current reused differential pair the input voltage is coupled to the gate and source terminals of the transistors through the coupling capacitors. With feedback resistor R_{f1}, the gate nodes of M_{N1} and M_{P1} coupled with positive input acts as shunt-feedback amplifier and with R_{f2} as load resistor, the source nodes of M_{N2} and M_{P2} coupled with positive input acts as CG amplifier. Since a SFB amplifier has negative voltage gain and a CG amplifier has positive voltage, SFBCG hybrid amplifier develops a differential output voltage. For the negative input, the device plays opposite roles. The voltage gain of the SFBCG hybrid amplifier is the summation of the gains of a SFB and CG amplifiers that is twice the individual current-reused SFB and CG differential amplifier.

$$A_V = \frac{2(g_{m,N} + g_{m,P})R_f - 1 + \frac{R_f}{r_o} + sR_f(C_{ds} - C_{gd})}{1 + \frac{R_f}{r_o} + sR_f(C_{gd} + C_{ds})} \qquad (2)$$

$$A_{V,DC} \approx 4 g_m R_f - 1 \qquad (3)$$

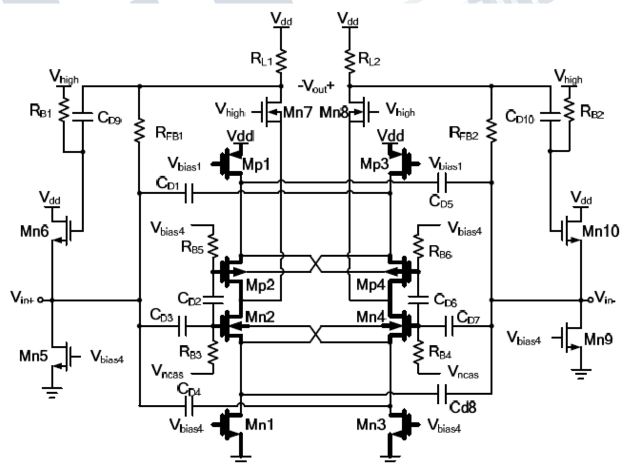

Fig.4. LNA circuit

B. LNA with active and passive feedback.

LNA utilizing a SFB amplifier combined with common gate amplifier including techniques back-gate coupling [2], current-reuse [8] and feedbacks is shown in Fig.4 [5].R_{FB1} and

R_{FB2} are the passive feedbacks used to reduce input impedance. Mn5, Mn6, Mn9 and Mn10 are the active feedbacks used that further reduce the input impedance. Passive and active feedback used in LNA effectively reduces the input impedance, chip area and save power consumption. Fig.5 shows the ac small signal model of the LNA. From the LNA ac small signal model gain of the amplifier can be obtained as

$$\frac{V_0}{V_{in}} = \frac{\frac{R_{eq}}{R_{FB1}}}{1 + SR_{eq}C_{L1}}(1 - 2G_mR_{FB1})$$

$$\cdot\left[1 + \frac{1 - G_mR_{FB1}}{1 + G_mR_{FB1}}\frac{sC_{GS,Mn7}}{G_{mMn7}}\frac{1}{1 - 2G_mR_{FB1}}\right] \quad (4)$$

Where Req = $R_{FB1}||R_{L1}$

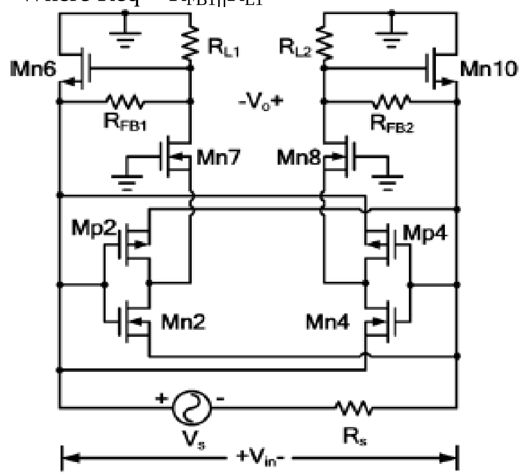

Fig. 5 LNA ac small signal model

Table 1. Results

Parameters	**Values**
PTM Technology	180nm
Frequency band	402M-405MHz
Gain	9.4dB
Noise Figure	7.4
OIP3	21dBm
IIP3	-18dBm
Input power	1.3mW

IV. CONCLUSION

This paper presents a Low Noise Amplifier for MICS band. Current-reuse, back-gate coupling and feedback techniques are adopted to enhance without extra power consumption. By applying these techniques. LNA achieves the required parameter values as shown in table 1. Simulations are done using H-SPICE using 180nm PTM Technology.

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