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A High Speed Performance and Low Power Consumption Design For VLSI Logic Circuits Using Multi-Threshold Voltage CMOS Technology

[1]Nisha S Police Patil [2] Swetha B
[1]PG Student, [2] Assistant Professor
RNSIT Bangalore-
[1]policenishapatil@gmail.com, [2]swetha26@gmail.com

Abstract: **Due to voltage scaling in CMOS logic circuits, there will be a reduction in threshold voltage which leads to increase in the sub threshold leakage current and hence static power dissipation. Although power consumption is important for modern VLSI design, the main requirements of the VLSI design are, operating speed and occupied area. Multithreshold voltage CMOS (MTCMOS) technology is a good solution providing high speed performance and low power design without area overhead. MTCMOS technology provides the transistors that have low, high and normal threshold voltage. The low threshold voltage transistors are used to reduce the propagation delay in critical (longest) path, the high-threshold voltage transistors are used to reduce the power consumption in shortest path. This paper describes a high-speed performance and low-power consumption design for full adder (using 2 half-adder), 4-bit ripple carry adder, 4x4 multiplier and 16-bit carry look-ahead adder circuits with MTCMOS technology using 45nm technology**

***Keywords*—Multi-threshold voltage CMOS (MTCMOS), static power consumption, propagation delay, sub threshold current.**

I. INTRODUCTION

Important consideration in the design of CMOS logic circuits is power dissipation. In the present deep-submicron era, the threshold voltages and power supply voltages for MOS transistors are greatly reduced. This is to an extent reduces the dynamic (switching) power dissipation. However, the sub-threshold leakage current increases exponentially thereby increase the static power dissipation. Leakage current is the current that flows through the off transistor i.e., transistor when it is switched off. It depends on gate length, oxide thickness and varies exponentially with threshold voltage, temperature and other parameters.

Power consumption is also crucial for deep DSM technologies. To further improve the performance of the circuits and to integrate more functions on a chip, the feature size has to continue to shrink. As a result, the power consumption per unit area grows, increasing the chip temperature. Since the dissipated heat needs to be removed to maintain an acceptable chip temperature, large cooling devices and expensive packaging are required in portable devices and high-performance digital systems such as microprocessors. Another important reason for low-power circuit design is reliability. As technologies continue to scale, not only does the power density increase, but also the current density increases.

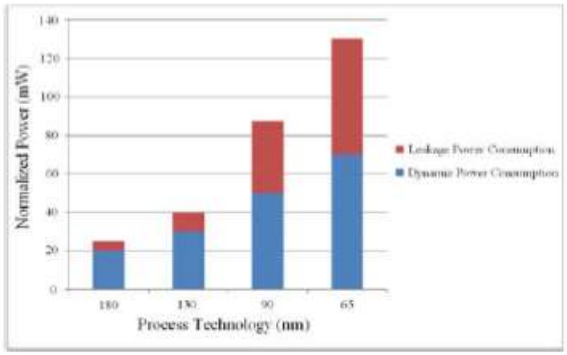


Fig. 1 Leakage and dynamic power consumption with technology scaling

Scaling down of threshold voltage VT results in exponential increase of the sub threshold leakage current. From the Fig.1 that its seen that leakage current is less compared to dynamic power for 180nm technology. When the scaling technology reached to 65nm, the leakage power is almost equal to the dynamic power. Hence, efficient leakage power reduction methods are very critical for the deep-submicron and nanometer circuits. Although power consumption is important for modern VLSI design, operation speed and occupied area are still the main requirements of the VLSI design. However, low-power

design usually involves making tradeoffs such as timing versus power and area versus power. Increasing performance, while the power consumption is kept constant, is also considered to be a low power design problem. To achieve high performance circuit design, MTCMOS technology is a good solution. In modern process technology, multi-threshold voltages are provided for each transistor. This paper describes high speed and low-power design for full adder (using 2 half-adder), 4-bit ripple carry adder, 4x4 multiplier and 16-bit carry look-ahead adder circuits with MTCMOS technology using 45nm technology.

II. MTCMOS TECHNOLOGY

Multi-threshold CMOS (MTCMOS) is a variation of CMOS chip technology which has transistors with multiple threshold voltages (VTH) in order to optimize delay or power. The VTH of a MOSFET is the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. Low VTH devices switch faster, and are therefore useful on critical delay paths to minimize clock periods[*clarification needed*]. The penalty is that low VTH devices have substantially higher static leakage power. High VTH devices are used on noncritical paths to reduce static leakage power without incurring a delay penalty. Typical high VTH devices reduce static leakage by 10 times compared with low VTH devices. One method of creating devices with multiple threshold voltages is to apply different bias voltages (Vb) to the base or bulk terminal of the transistors. Other methods involve adjusting the gate oxide thickness, gate oxide dielectric constant (material type), or do pant concentration in the channel region beneath the gate oxide.

A common method of fabricating multi threshold CMOS involves simply by adding additional photolithography and ion implantation steps. For a given fabrication process, the VTH is adjusted by altering the concentration of do pant atoms in the channel region beneath the gate oxide. Typically, the concentration is adjusted by ion\ implantation method. For example, photolithography methods are applied to cover all devices except the p-MOSFETs with photo resist. Ion implantation is then completed, with ions of the chosen do pant type penetrating the gate oxide in areas where no photo resist is present. The photo resist is then stripped. Photolithography methods are again applied to cover all devices except the n-MOSFETs. Another implantation is then completed using a different do pant type, with ions penetrating the gate oxide. The photo resist is stripped. At some point during the subsequent fabrication process, implanted ions are activated by annealing at an elevated temperature.

In principle, any number of threshold voltage transistors can be produced. For CMOS having two threshold voltages, one additional photo masking and implantation step is required for each of p-MOSFET and n-MOSFET. For fabrication of normal, low, and high VTH CMOS, four additional steps are required relative to conventional single- VTH CMOS. The most common implementation of

MTCMOS for reducing power makes use of sleep transistors. Logic is supplied by a virtual power rail. Low VTH devices are used in the logic where fast switching speed is important. High VTH devices connecting the power rails and virtual power rails are turned on in active mode, off in sleep mode. High VTH devices are used as sleep transistors to reduce static leakage power. The design of the power switch which turns on and off the power supply to the logic gates is essential to low-voltage, high-speed circuit techniques such as MTCMOS. The speed, area, and power of a logic circuit are influenced by the characteristics of the power switch.

III. CIRCUIT DESIGN USING MTCMOS TECHNOLOGY

MTCMOS technology provides a solution to the high performance and low power design requirements of modern designs. MTCMOS technology provides the transistors that have low, normal and high threshold voltage .This technology is an effective circuit level technique that provides a high performance and low-power design by utilizing both low and high threshold voltage transistors. Low-threshold voltage transistors have high-speed performance but high-power consumption. High-threshold voltage transistors have low power consumption but low-speed performance. While the low-threshold voltage transistors are used to reduce the propagation delay time in the critical path, the high-threshold voltage transistors are used to reduce the power consumption in the shortest path. This paper describes a low power and high speed design for full adder, 4-bit ripple carry adder and 4×4 multiplier and 16-bit carry look-ahead adder circuits with MTCMOS technology.

A. Design of full adder

A one-bit full adder is a combinational circuit that performs the arithmetic sum of three bits. It consists of three inputs A, B and CIN and two outputs Sum and Carry as illustrated in Fig. 2. Expressions for Sum and Carry are given as

$$Sum = A \oplus B \oplus Cin$$
$$Carry = AB + (A \oplus B)|Cin$$

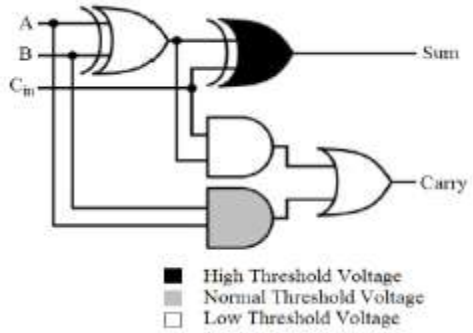


Fig. 2 Logic diagram for 1-bit full adder.

Use of low-threshold voltage transistors, normal-threshold voltage transistors and high-threshold voltage transistors in the circuit design. Since carry path is the longest path in the circuit, the low-threshold voltage transistors are used in this path to reduce the propagation delay time in the critical path. The second exclusive-OR gate present in the sum path is designed with high-threshold voltage transistors to reduce the power consumption in the shortest path. The remaining AND gate is designed with normal-threshold voltage- transistor.

B. Design of 4-bit ripple carry adder

A simple ripple carry adder (RCA) is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the carry output from each full adder connected to the carry input of the next full adder in the chain. Fig. 3 shows the logic diagram of 4- bit ripple carry adder. The 4-bit ripple carries adder contains 9 inputs (A0, A1, A2, A3, B0, B1, B2, B3 and Cin) and 5 outputs (Sum0, Sum1, Sum2, Sum3 and Carry)

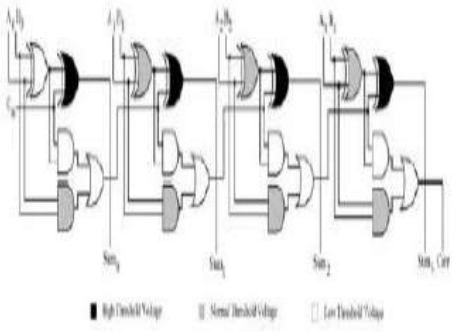


Fig. 3 Logic diagram of 4-bit ripple carry adder

For the ripple carry adder, Carry path is the longest path and the paths Sum0, Sum1, Sum2 and Sum3 are shorter when compared to the carry path. We use low-threshold voltage transistors, normal-threshold voltage transistors and high-threshold voltage transistors in the circuit design. Since carry path is the longest path in the circuit, the low-threshold voltage transistors are used in this path to reduce the propagation delay time in the critical path. The second exclusive-OR gates in each full adder cell are designed with high threshold voltage transistors to reduce the power consumption in the shortest paths. The remaining gates are designed with normal-threshold voltage transistors.

C. Design of 4×4Multiplier

The logic diagram of 4×4 multiplier is shown in the fig.4. The 4×4 multiplier circuit 8 inputs (a0, a1, a2, a3, b0, b1, b2 and b3) and 8 outputs (P0, P1, P2, P3, P4, P5, P6 and P7). The output P7 is the critical path (longest path) in this circuit. This critical path contains 2 half adders and 4 full adders as shown in the figure. The carry paths in each of these 6 adders are designed with low-threshold voltage transistors to reduce the propagation delay time in the critical path. The sum path in each of these 6 adders (the exclusive- OR gates in each of these 6 adders which gives the outputs P1, P2, P3, P4, P5 and P6) and the AND gate which gives the output P0 are designed with high-threshold voltage transistors to reduce the power consumption in the shortest paths. The remaining gates are designed with normal-threshold voltage transistors.

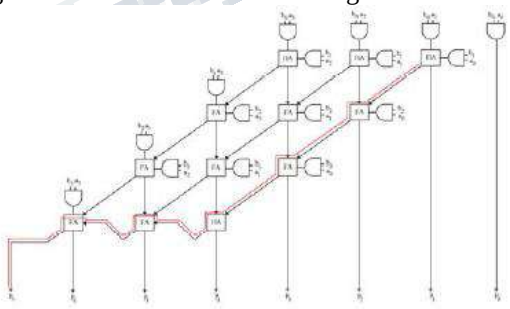


Fig. 4. Logic diagram of 4×4 Multiplier

D. Design of 16-bit carry look ahead adder

Fig 5 shows the block diagram of 16-bit carry look-ahead adder. The circuit is comprised of four 4-bit carry look-ahead adder blocks and a carry generator. We use low-threshold voltage transistors, normal threshold transistors, and high-threshold transistors in the circuit design. While the low-threshold voltage transistors are used to reduce the propagation delay time in the critical path, the high-threshold voltage transistors are used to reduce the power consumption in the shortest path. The normal-threshold transistors are used in other logic blocks.

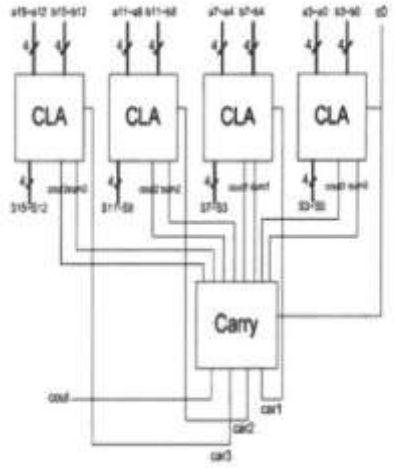


Fig.5. Block diagram of 16-bit carry look-ahead adder.

IV. RESULTS

The proposed full adder, ripple carry adder and multiplier circuits are simulated through HSPICE simulation using 45nm technology. The supply voltage for 45nm technology is 1.0V. Table 1 shows the comparison table between the conventional full adder circuit and the proposed circuit. The comparison between the conventional 4-bit ripple carry adder and the proposed circuit is shown in the table 2 and table 3 shows the comparison table between the conventional 4×4 multiplier circuit and the proposed circuit.

Table 1 Comparison table for full adder CIRCUI

	Conventional circuit	MTCMOS	% reduction
Static power (watts)	2.311E-5	1.764E-5	23.66%
Delay in critical path(sec)	2.599E-11	2.483E-11	4.46%

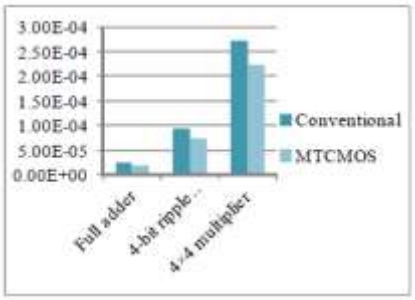
Table 2 Comparison table for 4-bit ripple Carry adder

	Conventional circuit	MTCMOS	% reduction
Static power (watts)	9.308E-5	7.292E-5	21.65%
Delay in critical path(sec)	6.814E-11	6.460E-11	5.19%

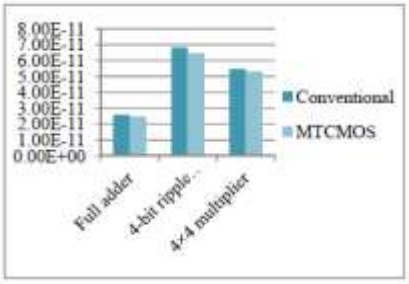
Table 3 Comparison Table For 4×4 Multiplier Circuit

	Conventional circuit	MTCMOS	% reduction
Static power (watts)	2.311E-5	1.764E-5	23.66%
Delay in critical path(sec)	2.599E-11	2.483E-11	4.46%

The proposed full adder circuit is achieved to reduce the power consumption by 23.66% and the propagation delay time by 4.46%. The 4-bit ripple carry adder is achieved to reduce the power consumption by 21.65% and the propagation delay time by 5.19%. The 4×4 multiplier is achieved to reduce the power consumption by 18.02% and the propagation delay time by 3.00%. Experimental results are shown in fig. 6.



(a) Static power



(b) Propagation delay

Fig 6: Results for full adder, ripple carry adder and 4x4 multiplier circuits for 45nm.

The proposed 16-bit carry look ahead adder is simulated through HSPICE simulation using the 0.35 um Samsung CMOS technology with a supply voltage of 3.3V. The verification of the layout of the circuit is performed through design rule check (DRC), electrical rule check (ERC) and layout versus schematic (LVS). Table 4 show the comparison table between the conventional CMOS circuit and proposed circuit. Conventional CMOS circuit used normal threshold voltage in all transistors has propagation delay time of 2.43 ns and power consumption of 1.36 mW. This circuit has propagation delay time of 2.39 ns and power consumption of 1.16 mW. Using ternary-threshold voltage CMOS transistors, the proposed circuit is achieved to reduce the power consumption by 14.71% and the power-delay by 16.1 1%.

Table 4 Comparison table for 16-bit carry Look-ahead adder

	Conventional circuit	MTCMOS	% reduction
Static power (watts)	1.36m	1.16m	14.71%
Delay in critical path (sec)	2.43n	2.39n	16.11%

V. CONCLUSION AND FUTURE DEVELOPMENT

The scaling down of device dimensions, supply voltage, and threshold voltage for achieving high performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. With deep-submicron and nanometer technologies, the leakage current becomes more critical in portable systems where battery life is of prime concern. MTCMOS yields better leakage reduction as the threshold voltage decreases and hence aids in further reduction of supply voltage and minimization of transistor sizes. Unlike other leakage control techniques, MTCMOS does not need any control circuitry to monitor the states of the circuit. Hence, MTCMOS avoids the sacrifice of obtained leakage power reduction in the form of dynamic power consumed by the additional circuitry to control the overall circuit states.

Here, low-power and high speed CMOS logic circuits are designed using MTCMOS technology. The propagation delay time in the critical path is reduced by using low threshold voltage transistors. The power consumption is reduced in the shortest path by using high-threshold voltage transistors. Since there is no additional circuitry added in this technique, there will be no area overhead to the proposed circuits. For 45nm technology, the proposed full adder circuit is achieved to reduce the power consumption by 23.66% and the propagation delay time by 4.46% compared to the conventional circuit. The 4-bit ripple carries adder is achieved to reduce the power consumption by 21.65% and the propagation delay time by 5.19% compared to the conventional circuit. The 4×4 multiplier circuit is achieved to reduce the power consumption by 18.02% and the propagation delay time by 3.00% compared to the conventional circuit. The 16-bit carry look ahead adder circuit is achieved to reduce the power consumption by 14.71% and the propagation delay time by 16. 1 % compared to the conventional circuit. Area of the various approaches using MTCMOS and design of various combinational and sequentially circuits using proposed method is to be estimated. The different techniques can be implemented in low power CMOS VLSI circuit to save the power dissipation increasing the battery life.

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