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An Efficient 4-Bit Processor Design Using Quantum Dot Cellular Automata Technology

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***Abstract*— Integrated Circuit(IC) fabrication technology is improving, so the internal dimension of semiconductor devices are decreasing day by day. This trend of scaling down dimensions reached its limit in near future. In nanoscale design, Complementary Metal Oxide Semiconductor (CMOS) has certain limitations such as hot electron effect, interconnect crosstalk, power dissipation, operating speed, gate oxide and interconnect scaling. According to the novel nanotechnology Quantum-dot cellular automata (QCA),which provides a better computation platform than traditional CMOS, in which polarization of electrons indicates the digital information. This work relies on an efficient 4 bit processor design based on QCA technology and it is compared with the CMOS technology. The processor mainly consists of a comparator, ALU, accumulator and data memory. The comparator were designed based on Tree-Based(TB) architecture, that is the entire bit is splitted into two halves and computed separately. Finally, it is cascaded together. The ALU consists of arithmetic operations such as full adder, full subtractor and logical operations such as AND and XOR. The data memory is a 4 *4 volatile memory. QCA based design reduces delay, power dissipation and number of cells used. The VHDL language is used for coding and synthesis can be done by means of Xilinx-ISE 13.2**

***Index Terms*— Accumulator, ALU, Comparator, Memory, Quantum Dot Cellular Automata (QCA)**

I. INTRODUCTION

The relentless evolution of electronics, communications , and information technology (IT) has been mainly enabled by progress in silicon-based complementary meta oxide semiconductor (CMOS) technology. This continuous progress has been maintained mostly by scaling its dimension, which results in exponential growth in both device density and performance. The economic productivity has been increased steadily due to the reduction in cost per function, with every new technology generation. Due to its scalability, the unique device properties such as high input resistance, self isolation, zero static power dissipation, layout and process steps have made CMOS transistors as the main components of the current integrated circuits (ICs). Today CMOS ICs are everywhere and necessary in our life, ranging from portable electronics to telecommunications and transportation.

Current CMOS technology is going to approach a scaling limitation in deep nanometer technologies. The CMOS technology in nanoscale experienced some problems due to increase in amounts of variation in every aspect for designing of nanometer. Quantum-dot cellular automata (QCA) is one of the promising new technologies for future generation ICs that overcome the limitation of CMOS. For this reason the design of logic circuits based on QCA has received a special deal of attention, and great efforts have been directed towards arithmetic circuits such as adders,comparators etc. The fundamental unit of QCA-based design is majority gate; hence, efficient construction of QCA circuits using majority gates has appealed a lot of attention.Since every QCA circuit can be implemented by using only inverter and majority gates. Inverter becomes another important component in constructing QCA circuits. The basic constituient of a nanostructure based on QCA is a square cell with four quantum dots and two free electrons. Due to Coulombic repulsion, the electrons will always reside in opposite corners ,thus leading to only two possible stable states, also named as polarizations. Locations of the electrons in the cell are associated with the binary states 1 and 0. Adjacent cells interface through electrostatic forces and tend to align their polarizations.

II. LITERATURE REVIEW

In nanoscale CMOS technology it has so many demerits. It is mainly found in channel, gate, drain or source and substrate.The Sub-threshold leakage current in the channel is the weak inversion conduction current, which is dominated by the diffusion current flowing between the drain and source. It is considered as one of non-ideal characteristics of MOSFET as a switching device and donates major portions of the standby leakage power dissipation[13]. The fundamental logic gates intrinsically available within the QCA technology are the inverter and the majority gate (MG). Three inputs a, b and c, the MG

performs the logic function. The first comparator design using QCA technology can verify only whether a = b. The device will assert its output only when the two inputs match each other[10].The second comparator design performs full comparator operation,but it operates only two single bit operands. The next comparator design is based on two 4-bit operands and it will performs the full comparator operation. This design will use Tree Based (TB) architecture that is,it will divide entire bit into two equal parts and performs the operations and finally cascaded together. The intermediate results obtained in this way are then further processed through a proper number of cateracted 2-input OR and AND gates implemented by means of MGs having one input permanently set to 1 and 0, respectively. The main drawback of this design is that it requires more majority voters (22) to perform the comparator operations,thus it consumes more area[6]. Single-bit full adder implemented with only inverters and majority voting logic gates. The device has three inputs:the operands A and Band the previous carry resultCi_1 . The two outputs are the sum S, and the carry bit Ci . Single bit full adders like this one can be easily chained together to produce a multibit adder. This full adder design uses five majority gates and three inverters[12].A bit-serial adder would perform the addition operation on two sequences of input bits (ai and bi for i = 1 to n) to generate a sequence of sum bits (Si for i =1 to n + 1). To be able to perform the addition operation, the adder would have to be capable of storing the intermediate carry bits. A feedback loop could be used to issue such storage. A bit serial adder containing three majority gates and two inverter gates and feedback control[12].The first full subtractor design using QCA uses four majority gates and two inverters[5].

III. PROPOSED SYSTEM

Quantum dot Cellular Automata (QCA) has attracted a lot of attention over the last two decades.QCA is an emerging technology and was introduced in 1993. QCA creates general computational functionality at the nano scale by simply controlling the posture of single electron. Circuits based on the QCA technology solve series of complications which the conventional devices face when it enters the domain of nano meter scale.

QCA consists of four charged quantum dots placed at the four corners of a square (cell).Each cell have two electrons, due to the columbic force of repulsion which are placed diagonally and the remaining two quantum dots are vacant. The tunnel helps the electron to move from one corner to other, thus helping in the flow of signal. There are two possible polarization states i.e. +1 and -1 depending on the emplacement orientation of the two electrons. The fundamental logic gate of a QCA is the Majority Gate and it has three inputs and the output will be equal to the maximum number of same state inputs.

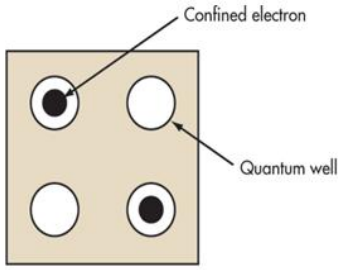

Fig.1 QCA cell representation

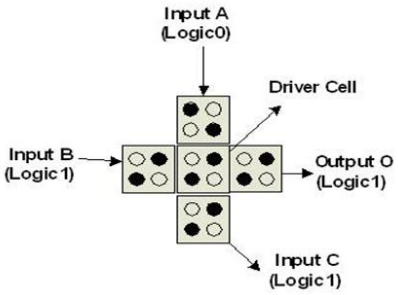

Fig.2 Majority Gate representation

The three inputs A, B and C then the logic function of majority gate can be represented as logical OR and logical AND functions can be contrapted from majority gate by presetting one of the inputs as +1 and -1 respectively. A QCA inverter helps a signal to invert and is called a logical NOT gate.

$$F = M(A;B;C) = AB + BC + CA \qquad (1)$$

TABLE I
TRUTH TABLE OF MAJORITY GATE

A	B	C	OUTPUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

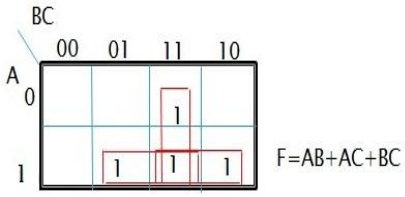

Fig.3 k-map simplification of majority gate.

Processor

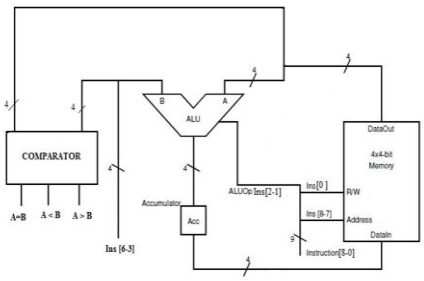

Fig.4 Block diagram of QCA based 4-bit Processor.

The block diagram describes a single processor,which operates 4-bit data. The design can be scaled to larger word lengths. The processor includes,Comparator, an ALU ,Memory and an Accumulator unit. The processor use a simple accumulator architecture.[9]

A. Comparator

In this each bit is compared and produce three outputs .i.e, greater than,less than,equal to. For this comparator design, it uses only majority gate and NOT gate. The operands A and B are preliminarily partitioned as A = $A_{MSB}A_{LSB}$ and B =$B_{MSB}B_{LSB}$. The portions A_{MSB} and B_{MSB} are compared independently of the portions A_{LSB} and B_{LSB}[1]. Consider two 4-bit numbers A(3:0)and B(3:0),and lets suppose that they are split into the subwords A(3:2), A(1:0), B(3:2) and B(1:0). If AbigB(3 : 2), AbigB(1 : 0), BbigA(3 : 2) and BbigA(1 : 0) are computed ,then AbigB(3 : 0) is equal to 1, if and only if A(3 : 0)bigB(3 : 0),whereas BbigA(3 : 0) is equal to 1, if and only if B(3 : 0)bigA(3 : 0).),if AbigB(3 : 0) and (BbigA(3 : 0)) are computed then is equal to 1 if and only if A(3:0)= B(3 : 0).

AbigB(3:0) = M(AbigB(3:2),(BbigA(3:2))',AbigB(1:0)) (2)

(BbigA(3:0))'=M(AbigB(3:2),(BbigA(3:2))',(BbigA(1:0))') (3)

AeqB(3:0) = M((AbigB(3:0))', (BbigA(3:0))', 0) (4)

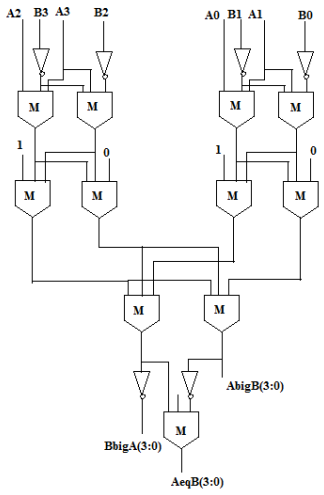

Fig.5 4-bit full comparator circuit diagram.

B. Arithmetic and Logic Unit(ALU)

The ALU performs the basic arithmetic operations such as full adder and full subtractor and that of logic operations such

as AND and XOR. Selecting particular operation by using a multiplexer.

Full Adder:

The proposed one-bit QCA adder structure that reduces the number of the majority gates and inverters required by existing designs.[7] A one-bit full adder is defined as follows:

Inputs: Operand bits a, b and carry-in cin.
Outputs: Sum bit S and carry-out Cout.

S = a.b.Cin + a '.b '.Cin + a '. b.Cin' + a.b '.Cin ' (5)

Cout = a.b + b.Cin + a.Cin (6)

By using the majority function , we get the QCA addition algorithm as

Cout = m(a, b, Cin) (7)

S = m(Cout ',Cin, m(a, b, Cin ')) (8)

The advantage of the recommended algorithm is that it simplifies the QCA addition. The calculation of Cout involves one majority gate and the calculation of S involves two majority gates and two inversion operations. The previous QCA addition algorithm , the calculation of Cout involves one majority gate and the calculation of S is that requires four majority gates and three inversion operations. The proposed design reduced hardware compared to the previous full adder designs.

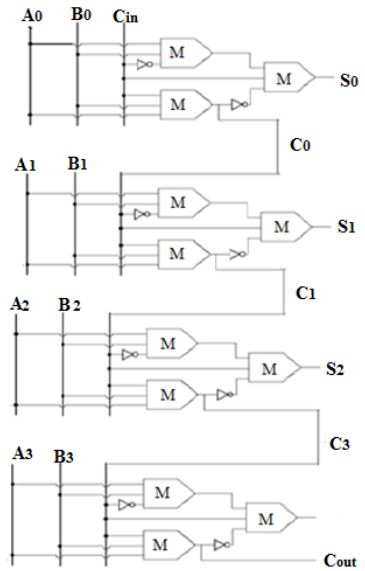

Fig.6 4-bit full adder circuit diagram.

Full Subtractor:

Full subtractor equation for difference and borrow [2].
Difference = A xor B xor C (9)
Borrow = A ' B + C'(A xor B) (10)

The characteristic equation of the full subtractor design can be written as
Borrow = m(A',B,C) (11)
Difference = m(m(A',B,C), m(A,B',C),C') (12)

The 4-bit full subtractor circuit diagram as below.

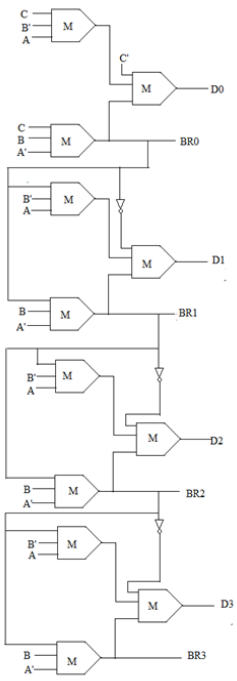

Fig.7 4-bit full subtractor

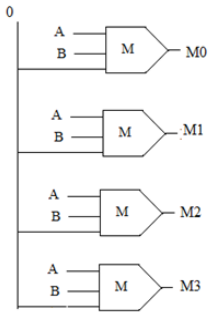

Fig.8 4-bit AND Operation

AND Operation:

The 4-bit AND gate circuit diagram is shown in the Fig.8. AND operation is performed using majority gate by setting any one of the input to 0.Using majority function the AND gate expression becomes:

M = m(a,b,0) (13)

XOR Operation:

Two-input XOR gate can be achieved using three majority voter gate and an inverter. Among these majority gates, two are made to act like AND gates by making one input line equal to 0 and the third majority gate acts like an OR gate by modeling the third input line equal to 1. The governing equation of XOR gate is simplified as follows[3]. Using majority function the output equation becomes,

W = m(m(a ',b, 0),m(a, b' 0), 1) (14)

The third input line of majority gate 1 is assembled high and that of majority gate 2 is assembled low. The output of majority gate 2 is fed into a not gate. Finally, the output from the majority gate 1 and that of the inverter is fed into majority gate 3 whose third input line is assembled to 0. The output of majority gate 3 is the XOR function.

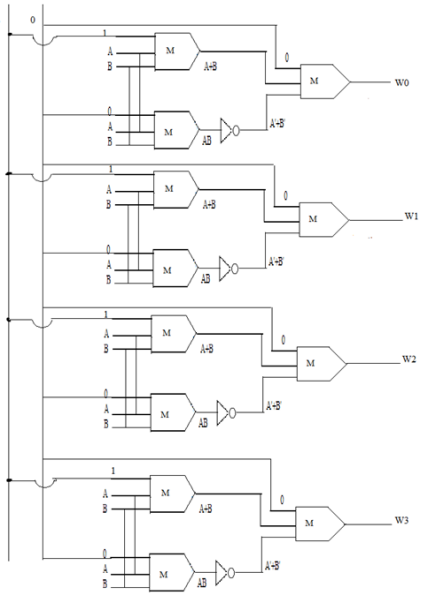

Fig.9 4-bit XOR Operation

5) *Multiplexer:*

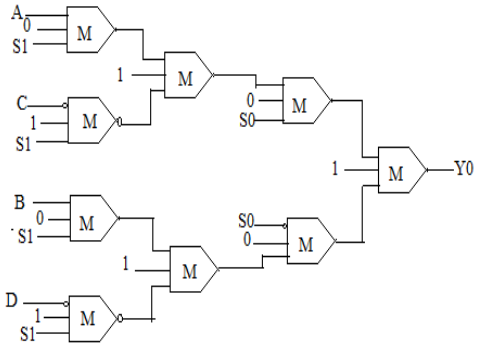

Fig.10 4:1 multiplexer

A 4:1 mux is having 4 inputs (A, B, C and D), two select lines (S0 and S1) and one output F. The expression of a 4:1 multiplexer can be written as,[4].

F = AS0S1 + BS00S1 + CS0S10 + DS00S10 (15)

Recommended design of QCA 4:1 mux is composed of 7majority voter gates. The inputs C and D are complemented
before it is applied to the minority gates. Both C and D inputs are ORed with the selection input S1 with a fixed polarization +1. The inputs A and B are applied to majority voter gates. Both A and B inputs are ANDed with the selection inputS1 with a fixed polarization -1.

C. Memory

In order to contribute the processor with data loading and storing capabilities, 4*4 SRAM are used as memory. Each SRAM cell includes a select line, read or write signal , an input data and an output data.

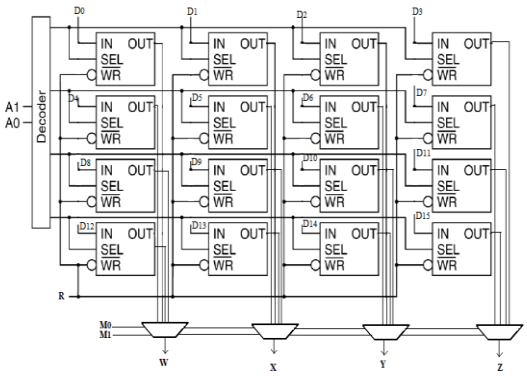

*Fig.11 Block diagram of 4*4 SRAM*

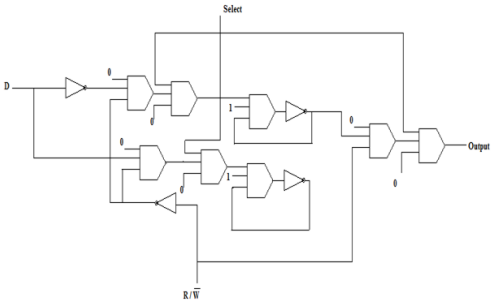

Fig.12 Single SRAM Cell

Static RAM is a type of RAM that embrace its data without external refresh, for as long as power is supplied to the circuit. This is distinctive to dynamic RAM (DRAM), which must be refreshed many times per second in order to hold its data contents. Memory chips include a decoder that metamorphose the address into the corresponding word in memory to be accessed. An AND gate is used to execute this decoding and there is one AND gate driving the enabling control line. The basic memory cell is a latch that is permitted by the select line going high. Static RAM is often used as cache memory in DRAM-based high performance computers. This magnifies their performance by storing previously accessed or written data, or storing the data in contiguous blocks of memory.

D. Accumulator

An accumulator is a register in which halfway arithmetic and logic results are stored. Without a register like an accumulator, it would be mandatory to write the result of each calculation to main memory. Access to main memory is slower than admittance to a register like the accumulator because the technology used for the large main memory is slower (but cheaper) than that used for a register.

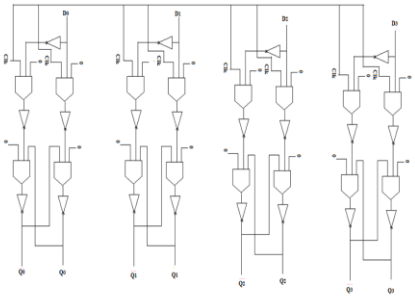

Fig.13 Accumulator logic diagram

IV. EXPERIMENTAL RESULTS

The modules are modeled and simulated using VHDL in Xilinx ISE Design Suite13.2.QCA processor has been designed and simulated and compare it with CMOS based processor.

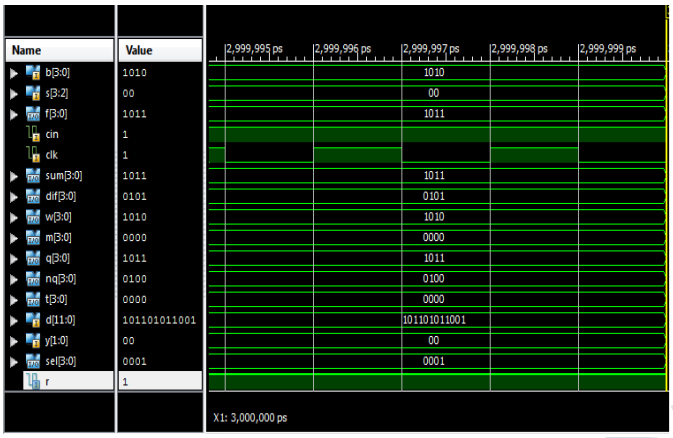

Fig.18 Simulation result of QCA based 4-bit processor

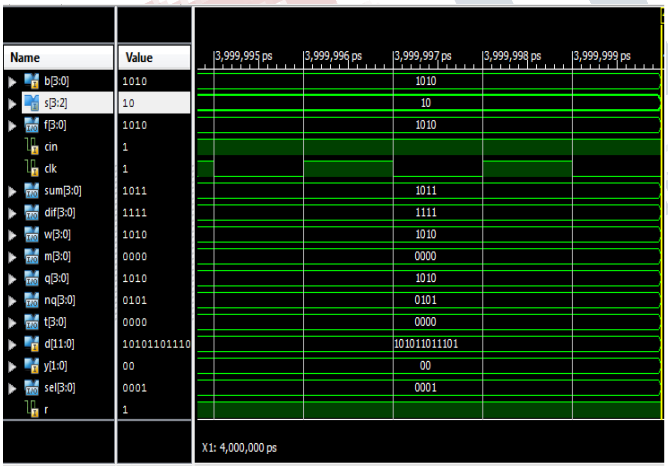

Fig.19 Simulation result of CMOS based 4-bit processor

TABLE II
COMPARISON BETWEEN CMOS AND QCA

Technology Used	Combinational Path Delay	Gate Count	Power Dissipation
CMOS	12.385nS	237	24mW
QCA	9.801nS	210	18mW

Comparison of CMOS and QCA Technology

QCA technology is better than CMOS technology.QCA technology consumes less power than CMOS technology ,and the combinational path delay is lesser in case of QCA technology .Comparatively the QCA technology posses less number of gate count than CMOS technology.

IV. CONCLUSION

CMOS technology has some limitations in nanoscale ,this limitations can be avoided by using the emerging technology QCA. A QCA based simple processor has been presented. Only half of the majority gates are used in the proposed comparator as compared to the existing QCA based comparator . It is based on innovative technology, that increased speed performances and reduces power dissipation. The comparison of QCA based processor , which shows the better efficiency than the CMOS technology. In future, QCA based 4-bit processor can be extended to higher word length.

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