ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 11, November 2016

Aging Aware Vedic Multiplier

[1] 1Ch.R.Sneha Sindhra [2] U.V. Ratna Kumari
[1]M.Tech Student, [2] Associate Professor,
JNTUK

Abstract: **-- Multipliers are most broadly utilized segment as a part of applications, for example, convolution, Fourier transforms, discrete cosine transforms, and advanced shifting. Since outrun of these applications primarily relies upon multiplier speed, multipliers must be composed effectively. The aging effect of the transistors caused by NBTI and PBTI has a large impact on its performance in a long span. In this paper, the device tradition with the accomplishment of Vedic multiplier is addressed not withstanding bypassing multiplier keeping as a main priority to enhance the execution for more speed and less power .The current plan focuses on Vedic multiplier which comprise of multi-level adders for designing mindful circuit. The huge angle of the proposed strategy is that, the created multiplier depends on Vertical and Crosswise structure of Old Indian Vedic Mathematics called Urdhava Tiryakbhyam Sutra. The advancement is to design the multiplier with the carry save adders in order to enhance better performance.**

***Index Terms*— NBTI, Vedic multiplier, Bypass multiplier, Urdhava Triyakbyam, Carry save adder.**

I. INTRODUCTION

Multipliers are the most significant units that are used in many applications, hence their design is of at most priority for the excelled performance of the computerized units. The two known effects that cause the aging of the multipliers are NBTI (Negative bias temperature instability) [2] and the PBTI(positive bias temperature instability).In short, NBTI effect is caused in the pmos transistor when there are accumulated traps in between oxide and silicon layers .These traps reduces the threshold voltage which makes the transistor on and so takes a while to switch on the transistor. Hence the increase in the threshold decreases the circuit speed. Meanwhile when the bias voltage is reduced, The reverse process takes place and the NBTI effect is unseen, but it shows a large impact in the long run. The corresponding effect in the nmos transistor is PBTI, which occurs when the nmos is under positive bias. It is observed that compared to the NBTI, PBTI is negligible [1]. A conventional technique to relieve from aging is overdesign including guard banding, gate over sizing. This approach can be exceptionally critical and power wasteful. To get out from this issue, numerous NBTI aware approaches have been proposed. One of such approach is variable latency adder design that is used in this paper. Here Vedic multiplier designed with carry save adder by using vertical and crosswise sutra is used along with the AHL (Adaptive Hold Logic. The detailed explanation of the Vedic multiplier, vertical and crosswise sutra, AHL circuit is given in the next sections.

II. PRELIMINARIES

Row Bypass Multiplier

This is a multiplier technique which is the improvement of the normal array multiplier[10], where the multiplier is consider as the primary element for the multiplication. The design includes (n-1)×(n-1) full adders, 2×(n-1)×(n-1) multiplexers, and 3×(n-1)×(n-1) three state gates[10]. The individual full adder circuit is shown in Figure:1

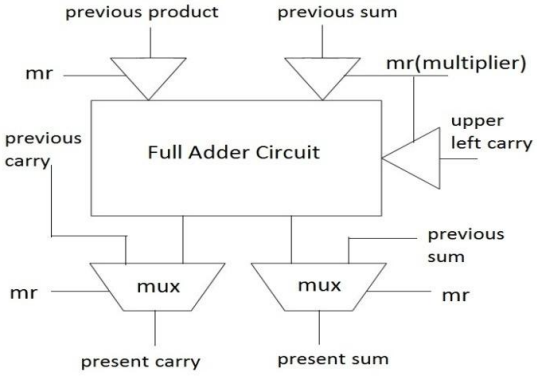

Figure 1: Structure of full adder (row bypass)

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 11, November 2016

Individual full adder circuit consists of three buffers, which are used at the input ports of the adder and two multiplexers at the output ports. The select line of both the buffers and the multiplexers is the multiplier bit. Depending on the multiplier bit, either the previous result is forwarded or the full adder operation is carried out. If the multiplier bit is 0, the previous result is forwarded, so that there occur no operation and if it is 1 , full adder circuit operates and gives the corresponding result. By this technique all the full adder circuits need not to be executed ,with multiplier bit 0. The power consumption can be reduced if one can reduce the switching activity of the logic circuit that is full adder circuits without changing its functionality

Column Bypass Multiplier

The multiplier in which the full adder operations are disabled if the corresponding multiplicand bit is 0. The design includes (n-1)×(n-1) full adders, 2×(n-1)×(n-1) multiplexers, and 2×(n-1)×(n-1) three state gates[10]. The multiplicand bit is used as the selector line for the multiplexer to decide the output of the full adder and also as a selector for the tristate gates to turn off the input path for the full adder. Figure:2 shows the individual full adder circuit of the column bypassing multiplier.

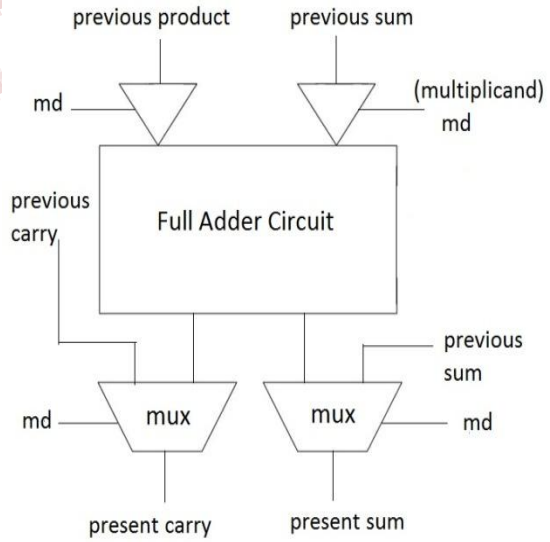

Figure 2: Structure of full adder (column bypass)

III. PROPOSED VEDIC MULTIPLIER

A. Vedic mathematics

Vedic mathematics is the ancient Indian system of mathematics[5] , part of four Vedas. Vedic mathematics comprises of 16 principles termed as sutras with which any mathematical operations can be done in a simple and fast manner. Paper presents a simple digital multiplier architecture based on the ancient Vedic mathematic sutra urdhva triyakbhyam also called vertical and crosswise sutra.

B. Urdhva Triakbyam

This sutra is the most prominent sutras of the Vedic mathematics where the calculations of the partial product and their sum are done in parallel[5]. Urdhva means up/down or vertical and Triyakbhyam means crosswise. This type of multiplier is most advantages as the bit number increases, the area and the gate size is partially increased as compared with other multiplier designs. This clock frequency independent multiplier uses area and power efficient technique[5]. Figure:3 illustrates the multiplication of the decimal numbers by using Urdhva Triyakbhyam sutra. The example includes multiplication of two decimal numbers 123 and 456.By using this technique output 56088 is obtained in an easy manner. Primarily the least significant bits of two numbers are considered as vertical for multiplication and then along with them the next bits in crosswise multiplication. In this manner all the bits are covered in vertical and crosswise format. Here the output is taken from bottom to the top while the carries added in the next steps in top down flow. This process is used for the binary numbers also.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 11, November 2016

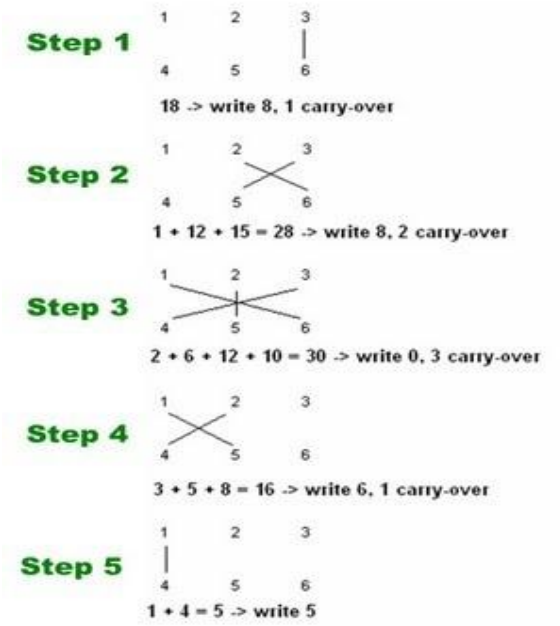

Figure 3 : Urdhva triyakbyam sutra

C. *Carry save adder*

One of the most fastest and the economic adder that do not propagate carry bits is the carry save adder. Historically, carry-save addition has been used for a limited set of intermediate calculations, with the most common example being the accumulation of the partial products of a multiplication[7]. It differ from other digital adders as it produces two different outputs ,one is the partial sum sequence the other is carry sequence. One normal adder is then used to add the set of carry bit to sum bits to give the final result of addition. The following Figure:4 depicts the 8bit Carry save adder.

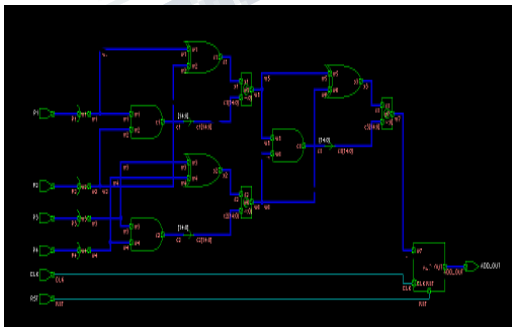

Figure 4 : Carry Save Adder

D. *Multiplier Using carry Save Adder*

Here, multiplier is designed by using the carry save adder[6]. Vedic multiplier (4x4) is shown in the Figure:5.It is implemented using four (2x2) Vedic multipliers and one 4 bit carry save adder and two 5 bit normal adder stages.

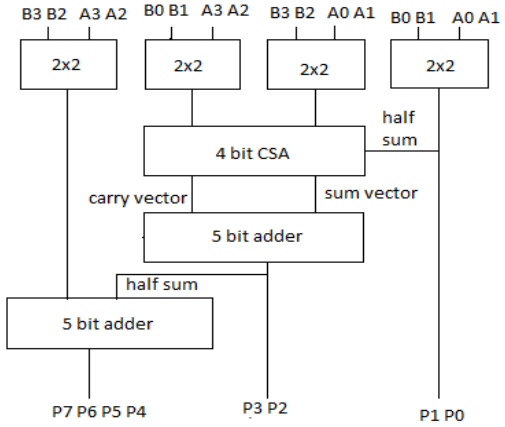

Figure 5 : Vedic Multiplier With CSA

The proposed multiplier makes use of 4 bit CSA and 5 bit adder circuits to produce the 8 bit result. The least significant bits of the two top level operands are driven into the right most (2x2)multiplier so that , it produces 4bit output out of which the right half product is given to the final product and the remaining half is padded with required amount of zeros and sent as initial carry to the 4 bit CSA. Next coming two (2x2) multipliers produce the output with the appropriate bits of the operands and are given to the 4 bit CSA. It gives the result , carry vector and sum vector, added using 5bit adder. Half sum of the 5 bit adder is retained for final product and the left over bits sent to other 5 bit adder with required padding. There it makes summation with the product from the left (2x2) multiplier and produces the result that is to be appended to the final product

IV. PROPOSED ARCHITECTURE MODEL

This section describes the aging model of the Vedic multiplier[8]. The architecture includes the Vedic multiplier with the (AHL) adaptive hold logic circuit and the razor FF[4] . Figure:6 depicts the architecture. It is a circuit with two m bit inputs and one 2m bit output. The work flow of the architecture is as follows:

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 11, November 2016

The inputs arrive at the Vedic multiplier and the adaptive hold logic circuit simultaneously. The Vedic multiplier computes the product of the input patterns and where as the AHL circuit determines whether the product generation require one cycle or two cycles depending up on the number of zero bits in the multiplier /multiplicand . Once the product is computed it is then given to the razor flip flop block where it determines whether the computed product met the timing violation or not. If it violates the timing the razor FF raises an error signal and indicate the AHL circuit to re execute.

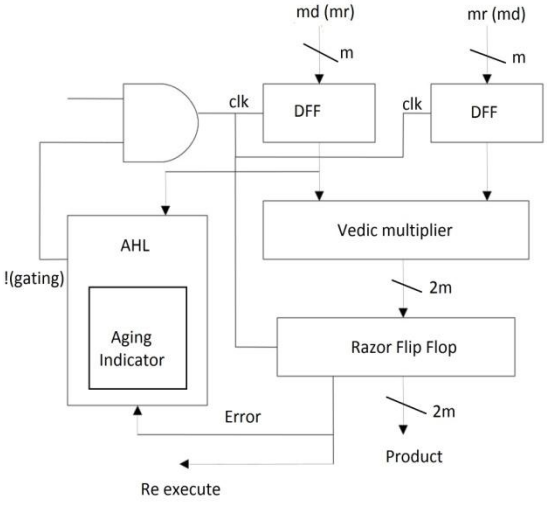

Figure 6 : Proposed Architecture

A. Razor flip flop

In this architecture razor FF determines whether the timing violation occurs before the next input pattern arrives. The 1bit razor flip flop consists of main flip flop, shadow latch, comparator and a multiplexer[4] shown in Figure:8. The main flip flop captures the result of the execution under the normal clock and where as the shadow latch captures at the delayed clock. Both the results of the main flip flop and the shadow latch is sent to the xor gate for comparison , the xor gate acts as comparator. If the latched bit is different from that of the main flip flop bit the comparator out is '1' and it is observed that the execution requires more than one cycle and the computed result is incorrect. When the comparator out is '1' , the razor flip flop raises an error signal. It is to be noted that each output product bit of the multiplier consists one razor FF block and the error signals from all the blocks are ORed together to the AHL block.

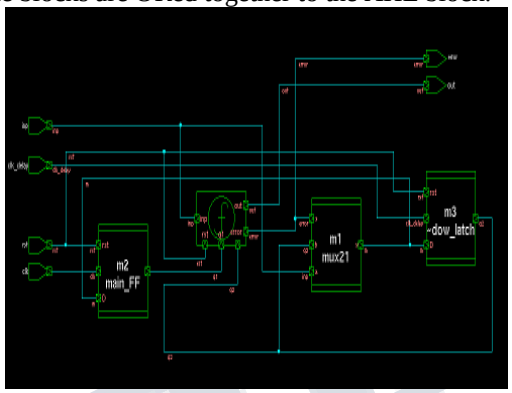

Figure 7 : Razor Flip Flop

B. Adaptive Hold logic

The AHL circuit is the key component of the architecture and it contains two judging blocks, multiplexer, aging indicator and a D flip flop[1]. The aging indicators indicates checks whether the circuit attain aging or not. It is just simply a counter that counts the number of error signals from the razor flip flop and resets once it reaches its ultimate.

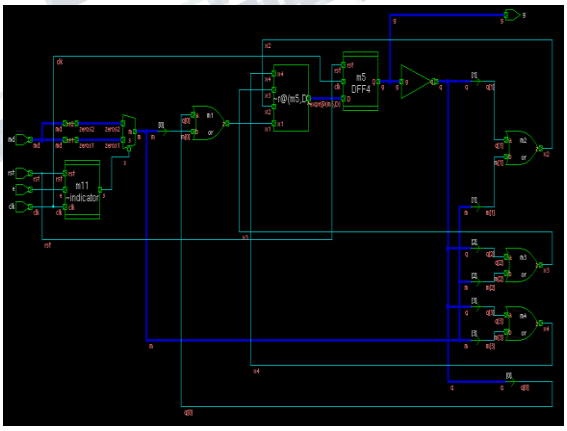

Figure 8 : AHL (Adaptive Hold Logic)

and it act as the select line for the multiplexer and the two judging blocks as the inputs. The two judging blocks determine the number of cycles required for execution depends on the zeros count. The first judging block with less number of zeros indicate it requires two cycles for execution and the second block

with more number of zeros requires one cycle for execution. The multiplexer selects one of either result based on the output of the aging indicator. Then an OR operation is performed between the result of the multiplexer, and the Q_signal is used to determine the input of the D flip-flop.

V. RESULTS

For the overall analyses of the Vedic multiplier using adaptive hold logic. The reduction in power and timing in compensation with area is observed. The analysis of the Vedic multiplier using AHL as compared the conventional bypass multipliers is done. By using AHL, the circuit minimizes the timing waste in the multiplier. So, it reduces the delay in the circuit. Table:1 depicts that the area, power and delay analyses for row bypass, column bypass and Vedic multipliers using AHL by simulation. The comparison proves that by the use of Vedic multiplier with AHL instead of by pass multipliers power and delay got reduced in compensation to area. In the future work, the Vedic multiplier can be designed by alternative sutra in the Vedic mathematics for even more better performance and even it can also be designed with different adder too.

Type of multiplier parameter	Row Bypass with AHL	Column Bypass with AHL	Vedic Multiplier with AHL
Area	**21.5nm**	**18.8nm**	**38.7nm**
Delay	**185ns**	**126ns**	**99.8ns**
Power	**692.6 uW**	**612.6 uW**	**432.2uW**

Table 1 : Comparison of various multipliers

REFERENCES

[1] Ing-Chao Lin, *Member, IEEE*, Yu-Hung Cho, and Yi-Ming Yang, Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic, IEEE transactions on VLSI Systems, Vol. 23, No. 3, March 2015.

[2] Dieter K. Schroder, Negative bias temperature instability: What do we understand? Microelectronics Reliability ,www.elsevier.com/locate/microrel 24 May 2006.

[3] Yu-Shih Su, Da-Chung Wang, Shih-Chieh Chang, *Member*, *IEEE*, and Malgorzata Marek-Sadowska, *Fellow*, *IEEE*, Performance Optimization Using Variable-Latency Design Style, IEEE transactions on VLSI systems, Vol. 19, NO. 10, October 2011.

[4] Dan Ernst, Nam Sung Kim, Shidhartha Das, Sanjay Pant, Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation, Proceedings of the 36th International Symposium on Microarchitecture 2003 IEEE.

[5] Poornima M, Shivaraj Kumar Patil, Shivukumar , Shridhar K P , Sanjay H Implementation of Multiplier using Vedic Algorithm International Journal of Innovative Technology and Exploring Engineering (IJITEE)ISSN: 2278-3075, Volume-2, Issue-6, May 2013.

[6] Gaurav Sharma, Arjun Singh Chauhan, Himanshu Joshi, Satish Kumar Alaria, Delay Comparison of 4 by 4 Vedic Multiplier based on Different Adder Architectures using VHDL International Journal of IT, Engineering and Applied Sciences Research (IJIEASR)Volume 2, No. 6, June 2013.

[7] Jasbir Kaur, Lalit Sood,Comparison Between VariousTypes of Adder Topologies IJCST Vol . 6, Issue 1, Jan - March 2015.

[8] Bandanadham bala kranthi kumar,Al. Shabana samantha tera, Design of an efficient aging aware reliable multiplier to reduce aging effects, International Journal of Computer Engineering In Research Trends , Volume 2, Issue 12, December-2015, pp.1070-1075.

[9] CH pavam moham , M suma ha, Realization of low power and area reduced aging aware multiplier design, International journal of electronic and electrical engineering and telecommunications, Vol. 4, No. 4, October 2015

[10] Nithya J, Sathiyabama G, Revathi K, Comparative Study of Low Power Low Area Bypass Multipliers for Signal Processing Applications, Int. Journal of Engineering Research and ApplicationsVol.5 Issue 1(Part 2), January 2015, pp.95-98 ..