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Implementation of Full Subtractor Circuit using Reversible Gates

[1] Anala M [2] Harsha M V
[1] Assistant Professor [2] PhD Research Scholar
[1] Department of ECE, K. S. School of Engineering and Management, Bangalore 560109.
[2] Department of ECE, University Visvesvaraya College of Engineering, Bangalore 560001.

***Abstract:* -- Reversible logic finds many applications, especially in the area of quantum computing. A specified n-input, n-output Boolean function is called reversible if it maps each input assignment to a unique output assignment and vice versa. The key objective of today's circuit design is to increase the performance without the proportional increase in power consumption. In this paper a full subtractor is designed using Feynman, Double Feynman and Fredkin gates.**

***Keywords*: Reversible Logic, Full Subtractor, Feynman gate, Double Feynman gate and Fredkin gate.**

I. INTRODUCTION

In the last decades, great achievements have been made in the development of computing machines. While computers consisting of a few thousands of components filled whole rooms in the early 70's, nowadays billions of transistors are built on some square millimeters. The number of transistors in a circuit doubles every 18 months (which is also known as Moore's Law) according to the founder of Intel, Gordon E. Moore, who formulated this as a prediction in 1965. Until today, this prediction has not lost any of its validity—each year more complexsystems and chips are introduced. Reversible logic marks a promising new direction where all operations are performed in an invertible manner. That is, in contrast to traditional logic, all computations can bereverted (i.e. the inputs can be obtained from the outputs and vice versa). This reversibility builds the basis for emerging technologies that may replace or at least enhance the traditional computer chip. Reversible system does not allow information to be erased. Thus the reversible gates have the same number of inputs and outputs which means that the input stage can always be retained from the output stage. Designing reversible circuits using reversible gates have several constraints:

a. The fan-out of every signal is equal to one.
b. Loops are not permitted in a strictly reversible system.

On the other hand, data shifting and rotating is important and frequently used in arithmetic operations, variable-length coding, bit-indexing and many more. In this consequence, barrel shifters which are capable of performing n-bit shifting and rotating of data in a single cycle, are normally used in embedded processors such as: digital signal processors and high performance processors, high-speed/low-power applications etc. Reversible circuits are interesting because the loss of information associated with irreversibility implies energy loss[4]. Reversible circuits can be viewed as a special case of quantum circuits because quantum evolution must be reversible. Classical (non-quantum) reversible gates are subject to the same "circuit rules," whether they operate on classical bits or quantum states.

II. PRINCIPLE OF REVERSIBLE LOGIC

Power dissipation is one of the important concerns in digital circuit design. As more and more logic elements are accommodated into smaller and smaller volumes and to clock them to very high frequencies then a lot of energy is dissipated. This energy loss can be stated by using Landeurs principle.

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That is the amount of energy dissipated for the loss of one bit of information is given by

Energy loss = KTln2 joules of energy (heat),

Where, K= 1.38x10^-23 joules (Kelvin)^(-1) is the Boltzmann's constant And T is the absolute temperature at which operation is performed[1]. Although the amount of heat dissipated at room temperature is very small, we cannot neglect this heat dissipation in CMOS circuits and quantum computing circuit design. If the revolution is continued in computer ALU performance we must continue to reduce the energy dissipated by logic operation, this can be done by improving the efficiency with which we can erase information. These are called reversible logic operations and Bennet showed that reversible circuits don't lose information due to one-to-one mapping between inputs and outputs hence no extra energy loss[2]. Summarizing, the synthesis of reversible circuits can be carried out from the input towards the outputs and vice versa.

III. SPECIAL TYPES OF REVERSIBLE GATES

Fredkin Gate: A 3*3 Fredkin gate output is given by the equation (A, B, C) where (P=A, Q = A'B+AC, R=A'C + AB) [6]. A 3x3 Fredkin gate is represented as shown in the figure1.

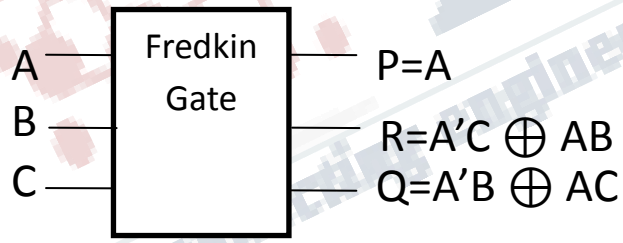

Figure1: Fredkin gate

K-CNOT Gate:

1. K=0:The 0-CNOT is just an inverter or NOT gate, and is denoted by N. It performs the operation (x (x XOR 1).

2. K=1:The 1-CNOT performs the operation (y , x) y , x XOR y). It is normally called as Feynman gate as shown in figure2 [5]. This is referred to as controlled NOT or CNOT or C.

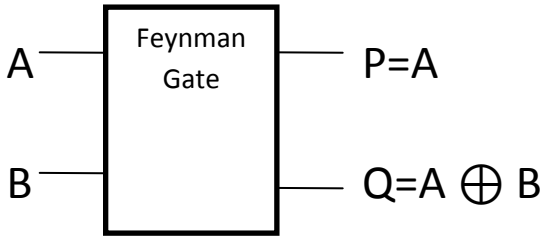

Figure 2: Feynman gate

3. K=2:The 2-CNOT is normally called a TOFFOLI (T) gate as shown in figure3 [6].

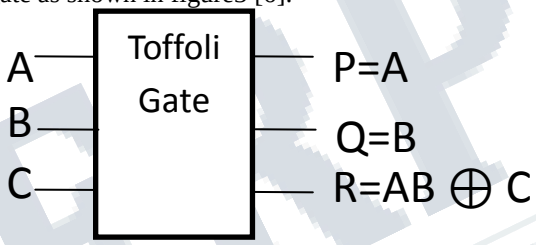

Figure 3: Toffoli gate

Swap Gate: Another reversible gate is shown in the figure4 called the SWAP (S) gate. It is a 2x2 gate which exchanges the inputs; that is (x , y) (y , x). The swap gate is also called TOFFOLI gate, same as 2-CNOT gate.

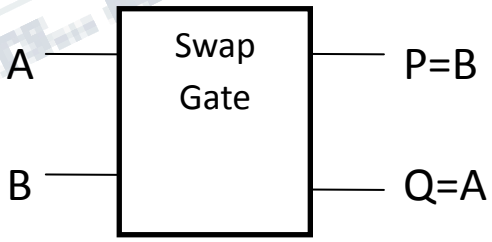

Figure 4: Swap gate

Peres Gate: A new permutation quantum gate is called as Peres gate [7]. It is a 3*3 gate with the equation P = A,Q= A XOR B, R = AB XOR C as shown in the figure5. It is combination of both Feynman and Toffoli gate form.

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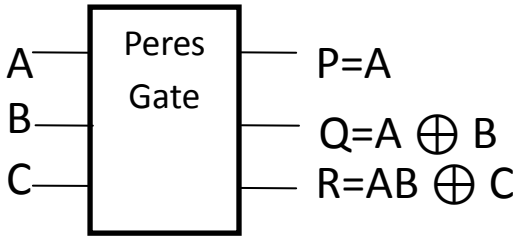

Figure 5: Peres gate

Double Feynman Gate (F2G): Figure6 shows the pictorial representation of 3×3 and R= A XOR C. Quantum cost of a Double Feynman gate is 2. It has three inputs (A, B, C) and three outputs (P, Q, R). The outputs are defined by P=A, Q=A XOR B, R= A XOR C.

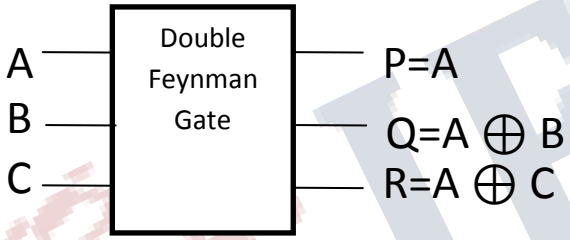

Figure 6: Double Feynman gate

MUX Gate: Figure7 shows the pictorial representation of 3×3 reversible MUX (MG) gate [3]. It has three inputs (A, B, C) and three outputs (P, Q, R). The outputs are defined by P=A, Q=A XOR B XOR C and R= A'C XOR AB. Quantum cost of a MUX gate is 4.

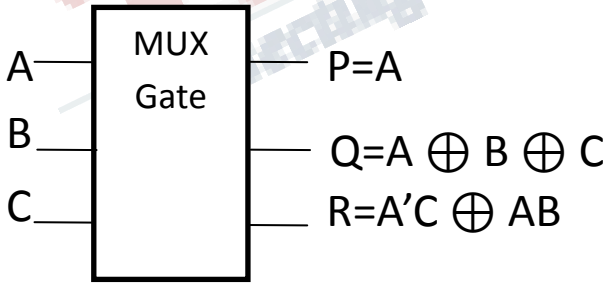

Figure 7: MUX gate

IV. BASIC DEFINITIONS OF REVERSIBLE LOGIC

***Definition 1*:** A multi-output function $f : Bn \rightarrow Bm$ is a reversible functionif

- Its number of inputs is equal to the number of outputs (i.e. $n = m$) and
- It maps each input pattern to a unique output pattern.

  A function that is not reversible is termed irreversible.

Definition 2: Quite often, irreversible multi-output Boolean functions should be represented by reversible circuits. This necessitates the irreversible function to be embeddedinto a reversible one which requires the addition of constant inputs and garbage outputs. A ***constant input***of a reversible function is an input that is set to a fixed value (either 0 or 1). A ***garbage output*** of a reversible function is an output which is a don't care for all possible input conditions.

***Definition 3*:** A well-formed reversible logic circuit is an acyclic combinational logic circuit in which all gates are reversible, and are interconnected without fan out. A reversible circuit has the same number of input and output wires; a reversible circuit with *n* inputs an *n*n* circuit, or a circuit on *n* wires.

Definition 4: The calculation of quantum cost (QC) has several approximations. Firstly the quantum cost of every 2*2 gate is the same and it is 1. Secondly, since each 1*1 gate can always be included to any 2*2 gate that precedes or follows it, the quantum cost of the 1*1 gate is considered to be zero. Thus every reversible gate is a combination of 1x1 or 2x2 reversible gate. So the quantum cost of a reversible circuit calculates the total number of 2*2 gates used.

V. SUBTRACTOR

A Combinational circuit which goes on performing subtraction of bits is known as subtractor. Subtractor are further classified into 2 parts

1) Half Subtractor:

Subtraction of two bits takes place in the half subtractor and two outputs are produced i.e. difference

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(D) and borrow (B).Figure 8 shows the systematic figure of half subtractor in which X and Y are input bits and D and B are output bits.

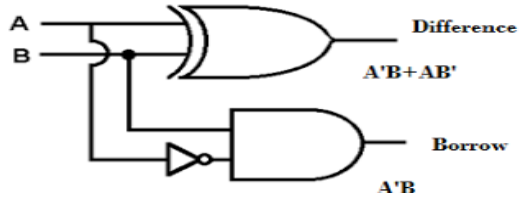

Figure 8: Half subtractor

2) Full Subtractor:

Full subtractor is the fundamental building block in many computational units. The full subtractor circuit's output is given by the following equations:

Difference=A⊕B⊕C
Borrow=A'B⊕A'C⊕BC

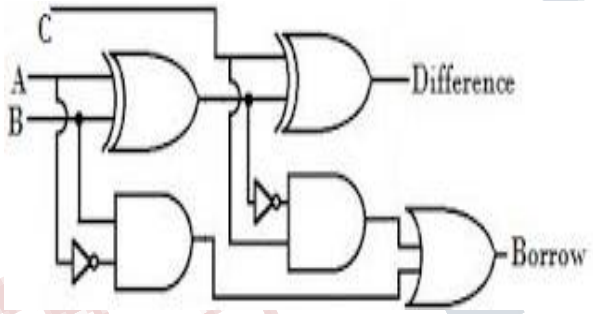

Figure 9: Irreversible full subtractor

Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table1: Truth table for full Subtractor

In full subtractor, subtraction of three bit is carried out i.e A, B, Bin and output difference and borrow(Bout) is produced. Figure9 below shows the systematic figure of full subtractor, in which two EXOR, two AND, two NOT and one OR gate is used in a specific combination.The truth table for full subtractor is shown in above table1.

VI. PROPOSED FULL SUBTRACTOR

In the existing literature, the reversible full subtractor is designed with 2 Toffoli gates, 3 Feynman gates and 2 NOT gates [8].

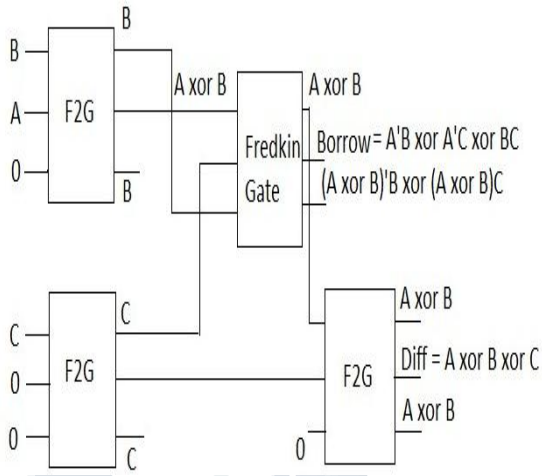

Figure 10: Reversible full subtractor circuit

The proposed reversible full-subtractor circuit is shown in figure10. This circuit is composed of 3 F2G gate and 1 Fredkin gate. It produces 4 garbage outputs and requires only one constant input. The quantum cost of F2G is 2 AND MUX is 4. So, the Quantum cost of this circuit is 10.

A.Quantum cost of 3 bit reversible full-subtractor:

In reversible full-subtractor, we have used 1 Mux gate and 3 Double Feynman gate. Now let m be the Quantum cost of MUX gate and D be the Quantum cost of Double Feynman gate. So, the Quantum cost of reversible full-subtractor is Quantum cost (FA) = 1m+3D

B.Total Logical calculation (T):
Assuming

α = A two input XOR gate calculation
β = A two input AND gate calculation
δ = A NOT gate calculation
T = Total logical calculation

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The Total logical calculation is the count of the XOR, AND, NOT logic in the output circuit. For example MUX gate has three XOR gate and two AND gate and one NOT gate in the output expression. Therefore (M) = 3α+2β+δ.and Double Feynman gate has two XOR gate .Therefore T (D) =2 α

VII. RESULTS OF FULL SUBTRACTOR CIRCUIT

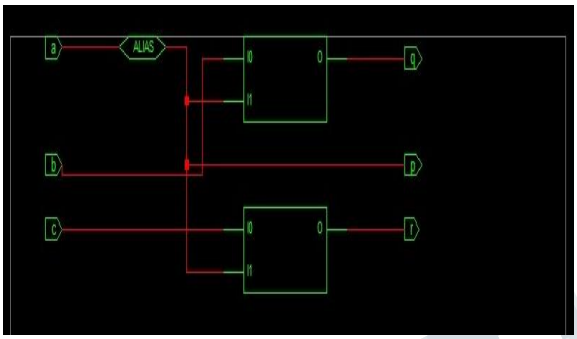

Figure 11: RTL Schematic of Feynman gate

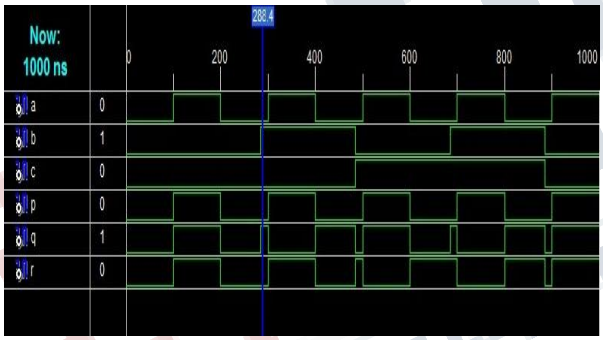

Figure 12: Simulation Waveform of Feynman gate

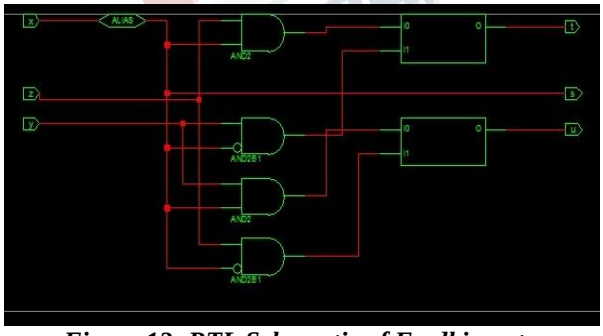

Figure 13: RTL Schematic of Fredkin gate

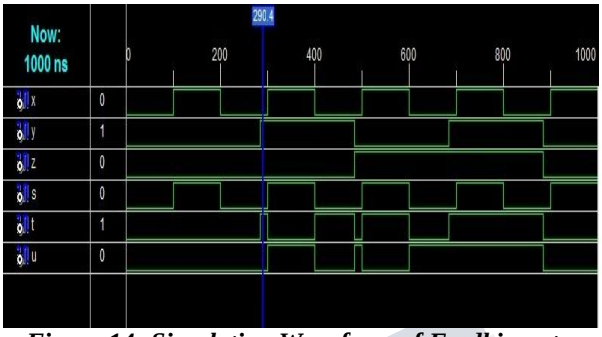

Figure 14: Simulation Waveform of Fredkin gate

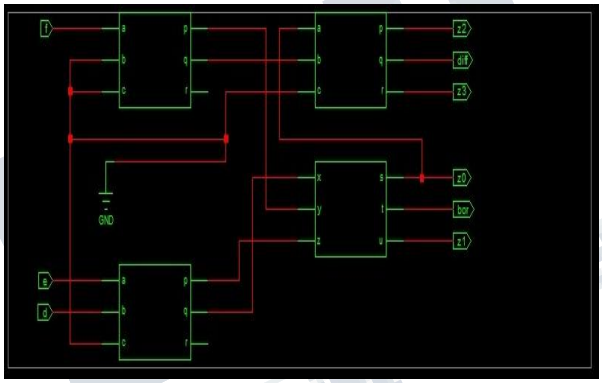

Figure 15: RTL Schematic of Reversiblefull subtractor

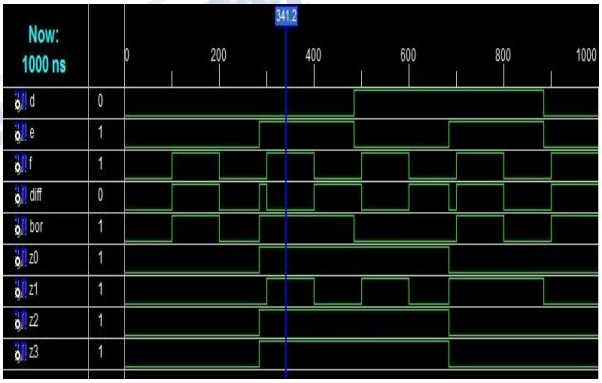

Figure 16: Simulation Waveform of Reversiblefull subtractor

VIII.CONCLUSION

This paper presents a cost efficient reversible full subtractor circuit. The full subtractors are mostly used for applications like Arithmetic and logical unit(ALU), Programme status word (PSW), Calculators, Embedded system, seven segment display

etc. This paper suggests the implementation of a new improved design of full Subtractor with the help of Double Feynman gate and MUX gate. The numerical results are also shown in the paper which shows the optimized results of the proposed design of combinational circuits against the previous ones and will provide a new arena to design digital logical systems.

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