International Journal of Engineering Research in Electronic and Communication Engineering (IJERECE) Vol 1, Issue 1, December 2014

# Low Power CMOS Based Dual Mode Logic Gates

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***Abstract*** **the advancement in technology and the expansion of mobile applications, power consumption has become a primary focus of attention in Very Large Scale Integration (VLSI) digital design. Recently digital sub-threshold circuit design has become a very promising method for ultra-low power applications. Circuits operating in the sub-threshold region utilize a supply voltage that comes close to or even less than the threshold voltages of the transistors, so it allows significant reduction of both dynamic and static power. A Dual Mode Logic (DML) gate, for selectable operation in either of static and dynamic modes. By scaling down the area there should be a need arise to scale down the supply voltage as well as threshold voltages of the device. It can cause static power dissipation to dominate dynamic power dissipation. To reduce the power consumption and dissipation of the circuit and increase the life time of the battery normally used in mobile phones and personal digital assistants Power Gated Sleep method can be applied. During sleep to active mode transition the stacked sleep transistors connected below the pull-down network are ON after a small duration. During the instant circuit should be experiences the Ground Bounce Noise (GBN). Inserting proper amount of delay which is less than the discharge time of the sleep transistor GBN will be reduced. The output of the circuit should be high enough to drive the another circuit. The simulations were done in TannerEDA 13.0 tool and power consumption of the proposed DML gates compared with Sleep and Dual Sleep methods in the 250-nm process.**

***Index Terms*****—Dual Mode Logic gates, Ground Bounce Noise, Sub-Threshold Region.**

## I. INTRODUCTION

In recent years the demand for low power devices has been increases tremendously. Low power consumption, speed of the system and the small area are the three main factors for increasing the performance. Reducing power dissipation is one of the most important issues in very large scale integration design today. As technology scales into the nanometer regime ground bounce noise and noise immunity are becoming important metric of comparable importance to leakage current, active power and area for the analysis and design of complex– arithmetic logic circuits. Static power consumption is a major concern in nanometer technologies. Along with technology scaling down and higher operating speeds of CMOS VLSI circuits, the leakage power is getting enhanced. Reduction in leakage power has become an important concern in low-voltage, low power, and high performance applications. This demand may be due to fast growth of battery operated portable applications such as cell phones, laptops and other handheld devices. There are three major components of power dissipation in complementary metal oxide circuits such as switching power, short circuit power and static power. Reducing any of these components will end up with low power consumption of the whole work.

## II. DUAL MODE LOGIC GATES

Dual mode logic (DML), designed to operate in the subthreshold region. The DML logic can be operated in two modes: static CMOS-like mode and dynamic np-CMOS-like mode (which will be referred to as a dynamic mode). In the static mode, the DML gates feature very low power dissipation with moderate performance, while in the dynamic mode, they achieve much higher performance with increased power dissipation. This unique feature of the DML provides the option to control system performance on-the-fly and thus support applications in which a flexible workload is required.

The basic DML gate architecture is composed of a standard CMOS gate and an additional transistor M1, whose gate is connected to a global clock signal, as shown in Fig. 1. The DML aims to allow operation in two functional modes: static mode and dynamic mode. To operate the gate in the dynamic mode, the Clock is assigned an asymmetric clock, allowing two distinct phases: precharge and evaluation. During the precharge phase, the output is charged to high/low, depending on the topology of the DML gate. In the consequent evaluation phase, the output is evaluated according to the values at the gate inputs. The DML topologies, marked Type A and Type B, are illustrated in Fig. 1.

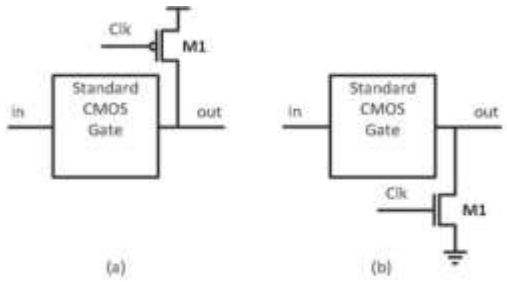


***Fig. 1. Proposed basic DML gate. (a) Type A topology. (b) Type B topology.***

Type A has an added p-MOS transistor that precharges the output to a logical "1" during the precharge phase. Type B has an added n-MOS that precharges the output to a logical "0". Dynamic logic gates are often implemented using a footer, which requires an additional transistor. The footer is used to decrease precharge time by eliminating the ripple effect of the data advancing through the cascaded nodes and allowing faster precharge. This is the key attribute to the immunity to process variations, temperature fluctuations, and solving some of the domino's well known drawbacks such as charge sharing, crosstalk noise, and susceptibility to glitches, which intensify with process and voltage scaling. DML shows high immunity to process variations, making it possible to operate DML gates from a supply voltage as low as 300 mV while operating in the dynamic mode, subthreshold DML achieves an improvement in speed of up to 10× compared to a standard CMOS, while dissipating 1.5× more power. In the static mode 5× reduction of power dissipation is achieved, compared to a basic domino, at the expense of a magnitude decrement in performance.

As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously. There are three major components of power dissipation in CMOS circuits: switching power, short circuit power and static power. Reducing any of these components will end up with low power consumption of the whole system. The first two components are referred to as dynamic power. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits. The current pulse from VDD to GND results in a short circuit dissipation. Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. The total power is given by the following equation

$$P_{total}=V_{dd}^{2}.F_{clk}.C_{load}+V_{dd}.\Sigma_i I_{isc}+V_{dd}.I_l \text{ ……. (1)}$$

where, Vdd is the power supply voltage, Fclk is the system clock frequency, Cload is the load capacitance, Iisc is the short-circuit current at node I and Il is the leakage current.

## III. GROUND BOUNCE NOISE

Ground bounce defines a condition when a device's output switches from high to low and causes a voltage change on other pins. It is usually seen on high density VLSI where insufficient precautions have been taken to supply a logic gate with a sufficiently low resistance connection to ground. Ground bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die. Essentially it is caused by a current surge passing through the lead inductance of the package. This voltage drop on the ground line creates two main problems: first it raises the chip off ground potential which in turn increases the devices input threshold level, and secondly increases the voltage level on an output pin which is not switching. This is also called Simultaneous Switching Noise. Fig. 2 shows the graphical representation of ground bounce noise.

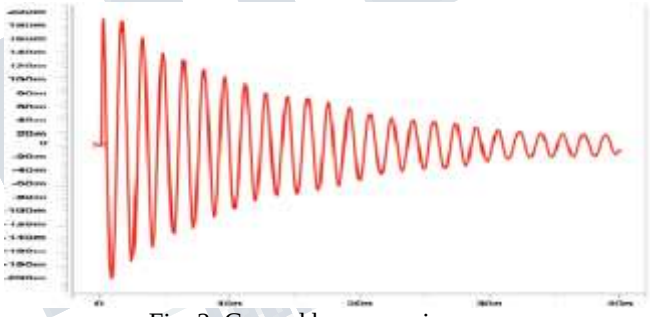

Fig. 2. Ground bounce noise

In this phenomenon, when the gate is turned on, enough current flows through the emitter-collector circuit that the silicon in the immediate vicinity of the emitter is pulled high, sometimes by several volts, thus raising the local ground, as perceived by the transistor, to a value significantly above true ground. Relative to this local ground, the base voltage can go negative, thus shutting off the transistor. Otherwise it is the large sudden current that flows through the power and ground rails during standby-to-active mode transition. This results in long period of power and ground rails' fluctuation, due to the inductance of the off-chip packaging and the on-chip power grids. This noise occurs in both power networks during mode transition, and the fluctuation in the power network. This GBN effect can be reduced by inserting proper amount of delay which is less than the discharge time of the sleep transistor.

## IV. POWER GATING TECHNIQUES

Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode [15]. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a

permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

Techniques for leakage power reduction can be grouped into two categories: state-preserving techniques where circuit state is retained and state destructive techniques where the current Boolean output value of the circuit might be lost. A state preserving technique has an advantage over a state destructive technique in that with a state-preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state. There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power. They are:

- Sleep method
- Dual sleep method

Each technique has its own merits and demerits. Based on the application, the technique which is best suited can be utilized.

### *A.Sleep Method*

In the sleep approach, a "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and a "sleep" NMOS transistor is placed between the pull-down network and Ground. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage. The circuit is connected as shown in Fig. 3.

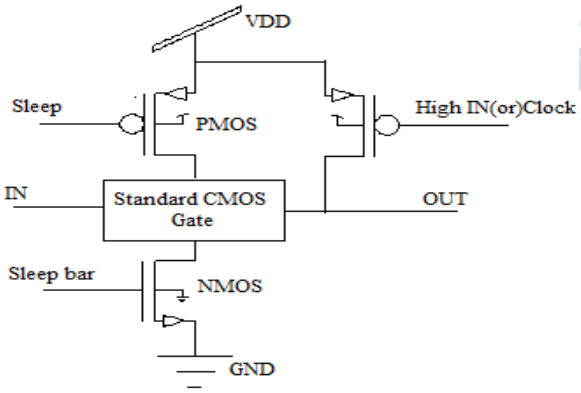


Fig. 3. DML Sleep method (Type A topology)

### *B.Dual Sleep Method*

Another technique called Dual sleep approach uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit. The sleep state attained due to the voltage headroom effect. The circuit is connected as shown in Fig. 4. The logic gates NAND, NOR and Inverter are implemented in these two methods and their average power consumption is measured for power comparison.

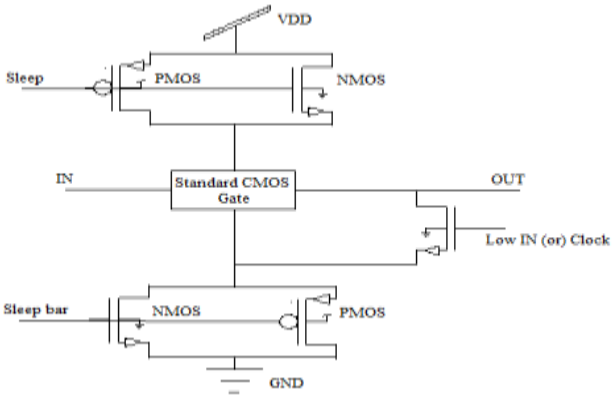


Fig. 4. DML Dual Sleep method (Type B topology)

## V. PROPOSED POWER GATED SLEEP METHOD

To reduce the power consumption of the circuit and increase the life time of the battery normally used in the devices, the sleep transistors are added. The PMOS sleep transistor is added in between $V_{dd}$ power rail and PMOS Logic network, NMOS sleep transistor is added in between NMOS logic network and ground. The sleep stacking is applied to sleep transistors. There are several benefits of combining stacked sleep transistors. First the magnitude of power supply fluctuations sleep mode during mode transitions will be reduced because these transitions are gradual. Second, while conventional power gating uses a high- threshold device as a sleep transistor to minimize leakage. Power gated sleep circuit has three modes of operations. They are,

1.Active mode
2.Standby mode
3.Sleep to active mode transition

In active mode, the sleep signal is held at '0' and sleep bar is '1'. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage. In standby mode operation sleep signal is held at '1' and the sleep bar signal is '0'. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage and leakage current is reduced by the stacking effect.

During sleep to active mode transition, the sleep transistor at the bottom side is turned ON after a small duration of time. According to the effect of GBN the output gets

oscillated. To make the circuit output stable desirable delay is applied to the sleep transistors by turning it off for a while. The GBN can be greatly reduced by controlling the intermediate node voltage VGND2 and operating the sleep transistor in triode region.

In stacking of transistors vary the threshold voltage of the transistors by providing bulk to source biasing negative. This increase the threshold voltage of the device, more threshold voltage means less sub threshold current, this cause less total leakage power. The threshold voltage of a device is given as,

$$V_{th} = 2\varphi_f + \left(\frac{\sqrt{2q\varepsilon N_a(2\varphi_f + |V_{bs}|}}{C_{OX}}\right) \quad \ldots\ldots\ldots (2)$$

where, $V_{th}$ is threshold voltage, $\varphi_f$ is built-in surface potential, $V_{bs}$ is body bias voltage, q is charge of an electron, $N_a$ is doping concentration and Cox is oxide capacitance.

### *A.Inverter*

In the DML Type A Power Gated Sleep Static Inverter topology, the switching element is a PMOS transistor connected parallel to the pull-up network. The input to the switching element is a constant high voltage is shown in Fig.5.

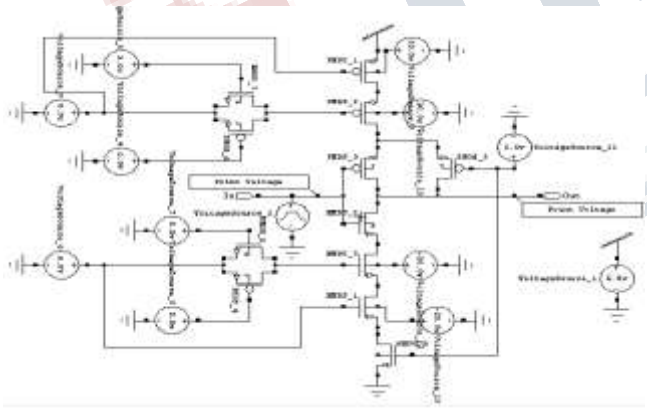

***Fig. 5. Type A Power Gated Sleep Static Inverter***

The footer is used to decrease pre-charge time by eliminating the ripple effect of the data advancing through the cascade and allowing faster pre- charge. The only difference when designing DML Type-A Power Gated Sleep Dynamic Inverter is that the input to the switching element is a clock signal.

In the DML Type B Power Gated Sleep Dynamic Inverter topology, the switching element is a NMOS transistor connected parallel to the pull-down network. The input to the switching element is a clock signal is shown in Fig. 6.The only difference when designing DML Type-B Power Gated Sleep Static Inverter is that the input to the switching element is a constant low voltage.

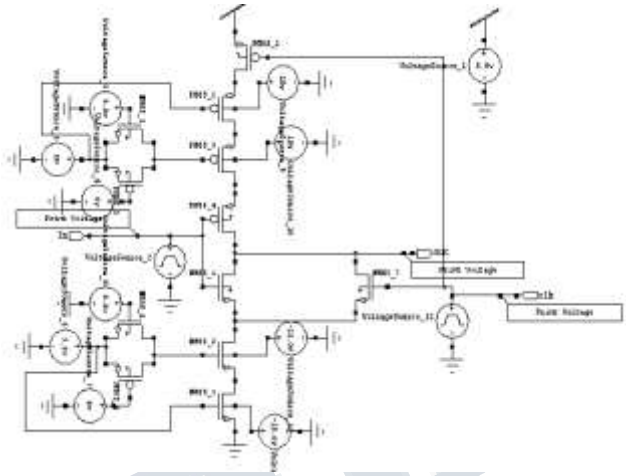

***Fig. 6. Type B Power Gated Sleep Dynamic Inverter***

### *B.NAND Gate*

In the DML Type-A Power Gated Sleep Dynamic NAND topology, the switching element is a PMOS transistor connected parallel to the Pull-up network. The input to the switching element is a clock signal is shown in Fig. 7. The only difference when designing DML Type-A Power Gated Sleep Static NAND is that the input to the switching element is a constant HIGH voltage.

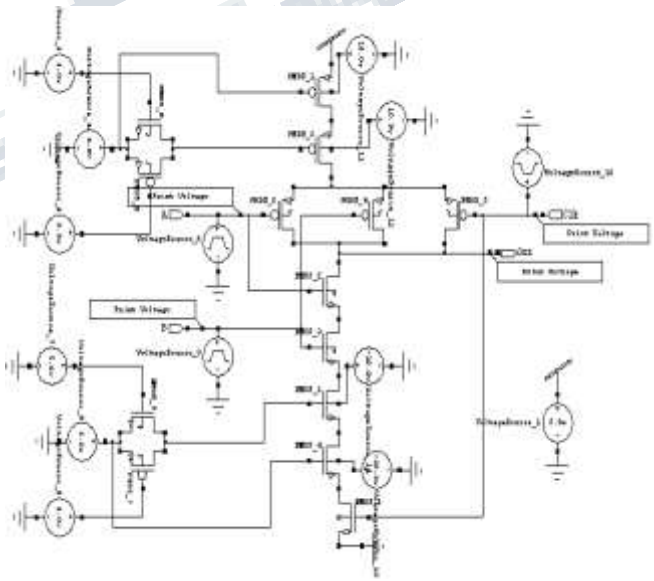

***Fig. 7. Type A Power Gated Sleep Dynamic NAND Gate***

In the DML Type B Power Gated Sleep Static NAND topology, the switching element is a NMOS transistor connected parallel to the pull-down network. The input to the switching element is a constant low voltage is shown in Fig.8. The only difference when designing DML Type-B

Power Gated Sleep Dynamic NAND Gate is that the input to the switching element is a clock signal.

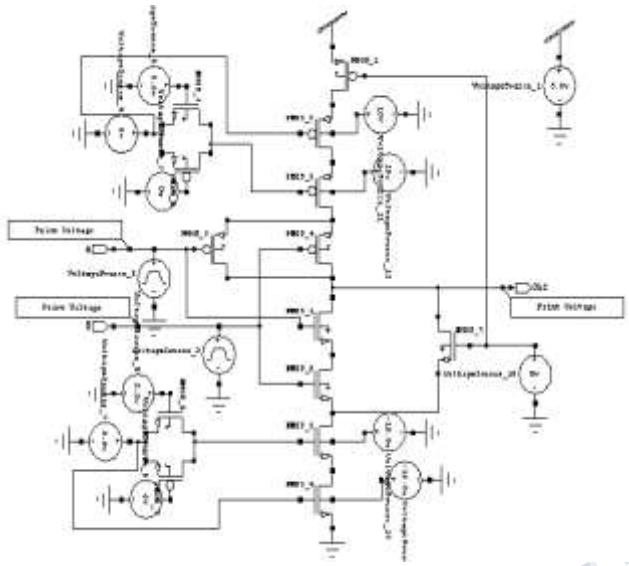

*Fig. 8. Type B Power Gated Sleep Static NAND Gate*

### *C.NOR Gate*

In the DML Type A Power Gated Sleep Static NOR topology, the switching element is a PMOS transistor connected parallel to the pull-up network. The input to the switching element is a constant high voltage is shown in Fig.9. The only difference when designing DML Type-A Power Gated Sleep Dynamic NOR Gate is that the input to the switching element is a clock signal.

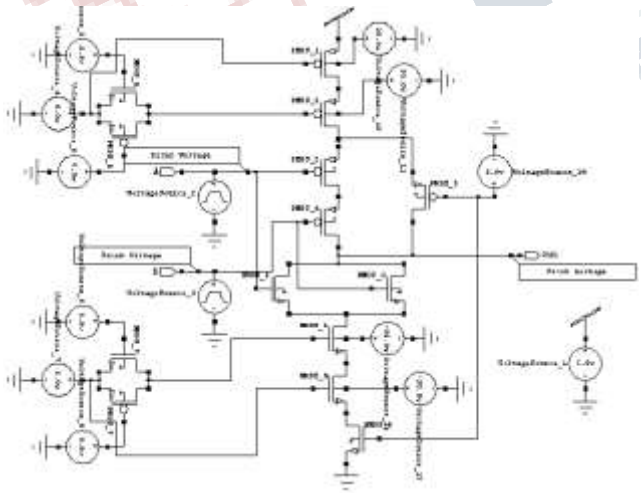

*Fig. 9. Type A Power Gated Sleep Static NOR Gate*

In the DML Type B Power Gated Sleep Dynamic NOR topology, the switching element is a NMOS transistor connected parallel to the pull-down network. The input to the switching element is a clock signal is shown in Fig. 10.The only difference when designing DML Type-B Power Gated Sleep Static NOR Gate is that the input to the switching element is a constant low voltage.

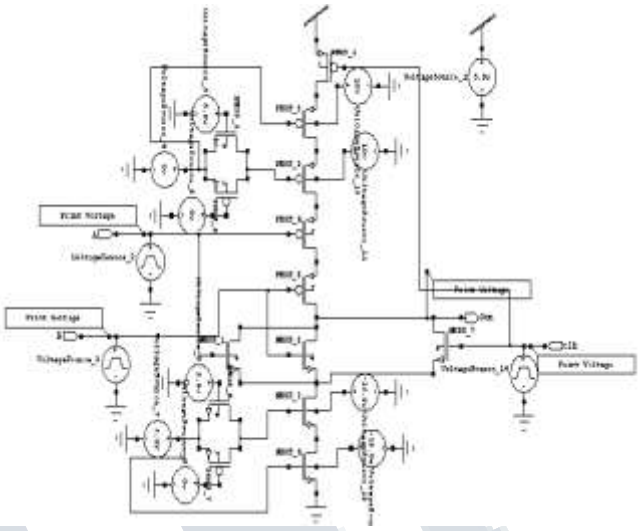

*Fig. 10. Type B Power Gated Sleep Dynamic NOR Gate*

## VI. SIMULATION RESULTS

The simulation is performed in Tanner EDA 13.0 at 250 nm technology. The operating temperature was maintained at 25ºC.The Output of Type A Power Gated Sleep Static Inverter is shown in Fig. 11.

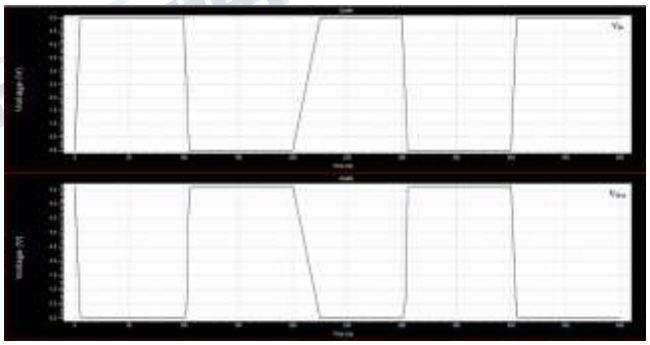

*Fig. 11. Output of Type A Power Gated Sleep Static Inverter*

The power gated sleep technique provides the output and the observed average power consumption is 5.546µW. For a supply voltage of 5V, the output of Type B Power Gated Sleep Dynamic Inverter is shown in the Fig. 12.

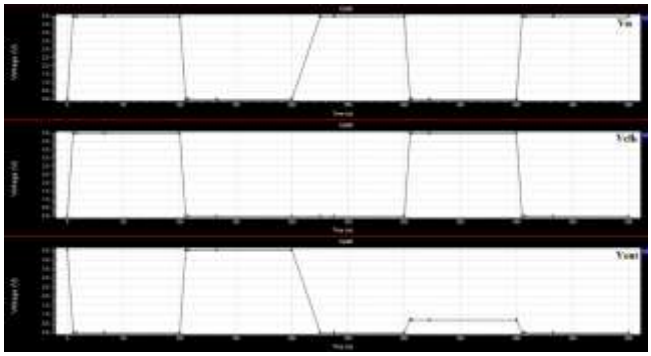

*Fig. 12. Output of Type B Power Gated Sleep Dynamic Inverter*

The power gated sleep technique provides the output and the observed average power consumption is 9.875µW. The Output of Type A Power Gated Sleep Dynamic NAND gate is shown in Fig. 13.

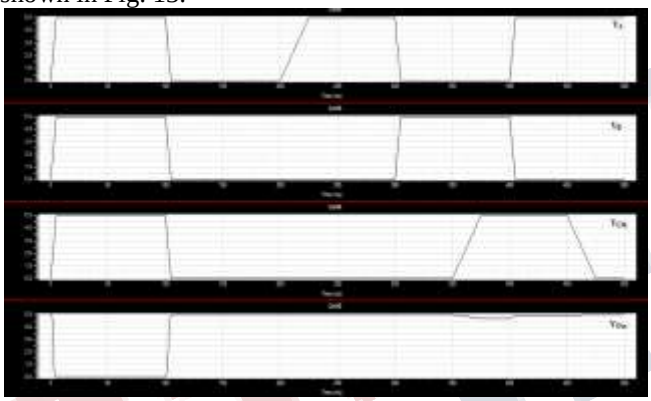

*Fig. 13. Output of Type A Power Gated Sleep Dynamic NAND gate*

The power gated sleep technique provides the output and the observed average power consumption is 14.347µW. For a supply voltage of 5V, the output of Type B Power Gated Sleep Static NAND is shown in the Fig. 14.

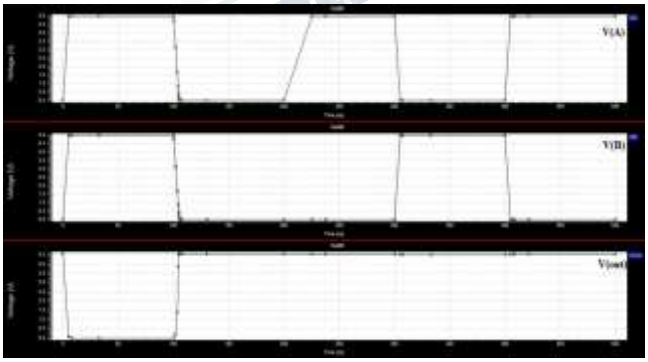

*Fig. 14. Output of Type B Power Gated Sleep Static NAND gate*

The power gated sleep technique provides the output and the observed average power consumption is 7.012µW. The Output of Type A Power Gated Sleep Static NOR gate is shown in
Fig. 15.

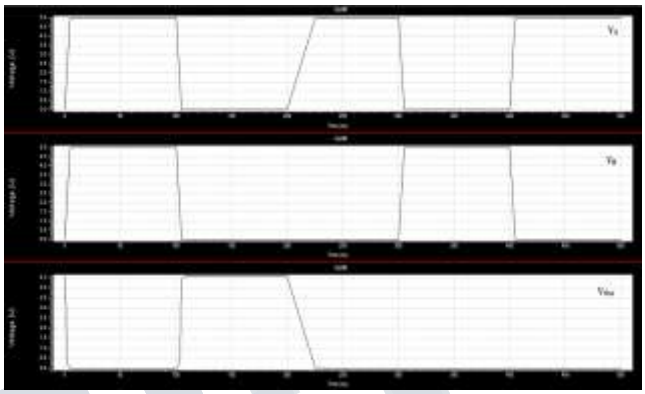

*Fig. 15. Output of Type A Power Gated Sleep Static NOR gate*

The power gated sleep technique provides the output and the observed average power consumption is 4.733µW. The Output of Type A Power Gated Sleep Static NOR gate is shown in Fig. 16.

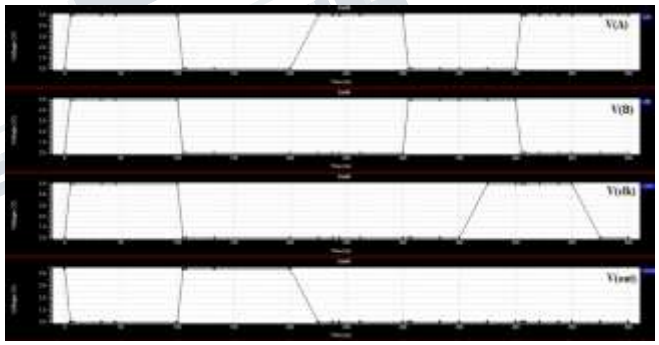

*Fig. 16. Output of Type B Power Gated Sleep Dynamic NOR gate*

The power gated sleep technique provides the output and the observed average power consumption is 12.080µW. Comparison of power consumed by Inverter, NAND and NOR gate are shown in Table I.II and III

**TABLE I**
**POWER COMPARISON OF INVERTER**

| Type | Sleep Method (µW) | Dual sleep method (µW) | Power gated sleep method (µW) |
|---|---|---|---|
| Type A Static | 4078.17 | 15.564 | 5.546 |
| Type A Dynamic | 77.451 | 17.451 | 9.173 |
| Type B Static | 17.754 | 16.785 | 9.653 |
| Type B Dynamic | 18.953 | 17.785 | 9.875 |

**TABLE II**
**POWER COMPARISON OF NAND GATE**

| Type | Sleep Method (µW) | Dual sleep method (µW) | Power gated sleep method (µW) |
|---|---|---|---|
| Type A Static | 44.64 | 44.52 | 13.529 |
| Type A Dynamic | 49.10 | 49.06 | 14.347 |
| Type B Static | 20.276 | 16.083 | 7.012 |
| Type B Dynamic | 22.626 | 17.240 | 9.437 |

**TABLE III**
**POWER COMPARISON OF NOR GATE**

| Type | Sleep Method (µW) | Dual sleep method (µW) | Power gated sleep method (µW) |
|---|---|---|---|
| Type A Static | 14.511 | 14.541 | 4.733 |
| Type A Dynamic | 16.104 | 16.130 | 5.202 |
| Type B Static | 14.212 | 13.414 | 10.485 |
| Type B Dynamic | 15.386 | 14.915 | 12.080 |

The power comparison of three methods tells us that the power gated sleep method provides optimal power consumption compared to other two methods.

## VII. CONCLUSION

In nanometer scale CMOS technology, sub threshold leakage power consumption is a great challenge. This paper presents a novel circuit structure named "power gated sleep method" as a new remedy for designer in terms of power products. The power gated sleep method shows the least speed power product among all methods. Therefore, the power gated sleep method provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. Especially it shows nearly 50-60% of power than the existing methods. So, it can be used for future integrated circuits for power Efficiency.

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