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Realization of Filter Bank Multi Carrier Processing using FPGA

[1] R.B.Aswathy, [2] S.Abinaya
[1] PG Scholar,Department of ECE,Mepco Schlenck Engineering College,Sivakasi
[2] PG Scholar,Department of ECE,Mepco Schlenck Engineering College,Sivakasi

Abstract: **- Filter Bank Multicarrier (FBMC) systems are a subclass of multicarrier (MC) systems. While its basic principle is dividing frequency spectrum into many narrow sub-channels. Filter Bank multicarrier aims to overcome the shortcomings that were encountered with the OFDM, Orthogonal Frequency Division Multiplexing. Field- Programmable Gate Arrays (FPGA's) are especially suited to fulfill these requirements. FPGA's are very powerful, relatively inexpensive, and adaptable since their configuration is specified in an abstract hardware description language. The aim of this work is to design a receiver side of FBMC in FFT and pipelined FFT structure with improved throughput, BER, and bandwidth range using Verilog HDL and implement it on FPGA. Here the results are obtained using MATLAB and Verilog HDL implemented on Spartan-6 FPGA board. The result of FFT and the pipeline FFT with timing summary is computed and the performance of FBMC is improved by adding the FIR filter at the receiver side. Filters usually low pass filters are uniformly spaced and are higher in selectivity to achieve minimum crosstalk.**

Keywords: **Fast Fourier Transform (FFT), Filter Bank Multicarrier (FBMC), Orthogonal Frequency Division Multiplexing (OFDM), Field Programmable Gate Array (FPGA).**

I. INTRODUCTION

Orthogonal frequency-division multiplexing (OFDM) is a method of encoding digital data on multiple carrier frequencies. Conceptually, OFDM is a specialized FDM, the additional constraint being that all carrier signals are orthogonal to one another. In OFDM, the sub-carrier frequencies are chosen so that the sub-carriers are orthogonal to each other, meaning that cross-talk between the sub-channels is eliminated. Since OFDM has some drawbacks as Sensitive to Doppler shift, Sensitive to frequency synchronization problems. High peak-to-average-power ratio (PAPR), requiring linear transmitter circuitry, which suffers from poor power efficiency. Loss of efficiency caused by cyclic prefix/guard interval. To overcome the shortcomings FBMC is used.

A. FBMC

FBMC is a new waveform technique having few advantages over OFDM a contender for 5G. For correct detection, multiple access interference (MAI) cancellation should be performed at the receiver in OFDM. MAI is suppressed due to the excellent frequency localization of the subcarriers in FBMC. Cyclic Prefix extension required and therefore reduces Bandwidth (BW) efficiency in OFDM. Not required and hence conserves BW in FBMC. Large side lobes in OFDM compared to FBMC for frequency spectrum. Highly sensitive to the carrier frequency offset in OFDM. Less sensitive and hence performs significantly with the increase of the user mobility in FBMC. Degraded spectrum sensing performance due to the spectral leakage in OFDM signals. High spectrum sensing resolution in FBMC. FBMC can support asynchronous sub bands and it has more spectral efficiency than OFDM. FBMC helps to eliminate the defect of mobility synchronization and reduce the wastage of resource spectrum bandwidth of Orthogonal Frequency Division Multiplexing (OFDM) in 4G communication.

B. FILTERING EFFECT OF FFT STRUCTURE

The FFT is running at the rate of the serially transmitted samples. The relationship between the input of the FFT and the output with index k = 0 is given as

$$y0(n) = \frac{1}{M}[x(n-M) + \cdots + x(n-1)]$$

$$y0(n) = \frac{1}{M}\sum_{i=1}^{M} x(n-i) \quad \text{——} \quad (1)$$

Where, y0 (n) is the output of FFT
M is the number of coefficients
x(n) is the input of FFT

Equation (1) is a low-pass linear phase FIR filter with the M coefficients equal to 1/ M .

$$I(f) = \frac{\sin\pi fM}{M\sin\pi f} \quad \text{——} \quad (2)$$

Where I(f) is the frequency response

In eqn (2), delay constant is said to be ignored. An FIR filter can be defined by coefficients in the time domain or by coefficients in the frequency domain. The two sets of coefficients are equivalent and related by the discrete Fourier transform (DFT).In the terminology of filter banks, the first filter in the bank, the filter associated with the zero frequency carrier, is called the prototype filter,

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because the other filters are deduced from it through frequency shifts

II METHODOLOGY

The addition of Cyclic Prefix (CP) in OFDM results into reduction of spectral efficiency and hence it is not favorable for multicarrier uplink as well as cognitive radio system. Hence desired bandwidth efficiency along with spectral efficiency can be achieved in FBMC. Instead of cyclic prefix, digital filters are used then the structure is said to be FBMC which is the major difference between the OFDM and FBMC as shown in Figure (1). Filters usually low pass filters are uniformly spaced and are higher in selectivity to achieve minimum crosstalk.

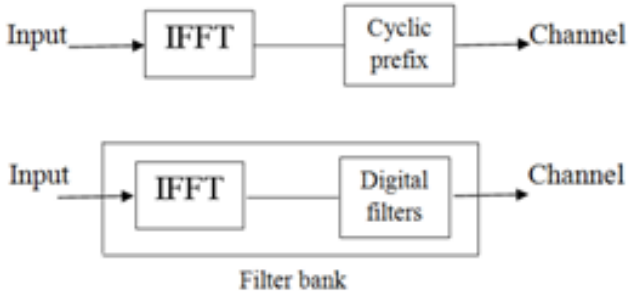

Figure 1. OFDM and FBMC Transmitter

A. FBMC

Filter Bank Multicarrier (FBMC) technique is recognized as one of the potential scheme that is capable of resolving some of the major problems associated with other multicarrier communication techniques like Orthogonal Frequency Division Multiplexing (OFDM).The Side-lobe variations of OFDM and FBMC structure is shown in Figure (2). Basic design principles are used for that purpose, recognizing FBMC scheme as an extension to OFDM as well as a separate transmission technique. In addition, increase of throughput in a spectrally efficient manner over other wireless transmission systems is one of the supplementary main aspects addressed by this scheme. This is considered as a crucial objective in order to meet the demand arisen from the ever increasing number of users, upcoming applications and rapidly evolving services. Starting from verification of basic formulation, performance of causal multirate FBMC technique is investigated. Due to the disadvantages and limitations associated with existing multicarrier communication techniques in the family of OFDM techniques, FBMC is considered as a possible alternative technique. Transmit signal equation for FBMC is

$$X(t)= \sum n \sum_k Sk(n) Pk(t - \frac{nT}{2}) \quad \text{——} \quad (3)$$

Where,

$$Pk(t) = P(t)e^{j(k+n)\pi/2}e^{j\pi kt/T} \quad \text{——} \quad (4)$$

X(t) is the transmit signal of FBMC
T is the instantaneous time with respect to t
Sk(n) is the sampling signal

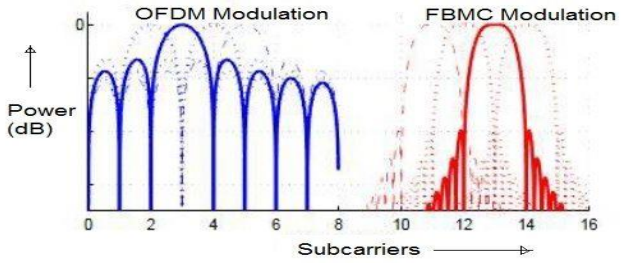

Figure 2 Side-lobes of OFDM and FBMC

B. QPSK MODULATOR

QPSK modulator is also known as quadric phase PSK, 4-PSK, or 4-QAM. QPSK uses four points on the constellation diagram, equi-spaced around a circle. With four phases, QPSK can encode two bits per symbol as shown in Figure (3). The mathematical analysis shows that QPSK can be used either to double the data rate compared with a BPSK system while maintaining the same bandwidth of the signal, or to maintain the data-rate of BPSK but taking half the bandwidth needed. The BER of QPSK is exactly the same as the BER of BPSK .The transmitted carrier can undergo numbers of phase changes.

Table 1 Constellation table for QPSK

$b(n), b(n+1)$	I	Q
00	$1/\sqrt{2}$	$1/\sqrt{2}$
01	$1/\sqrt{2}$	$-1/\sqrt{2}$
10	$-1/\sqrt{2}$	$1/\sqrt{2}$
11	$-1/\sqrt{2}$	$-1/\sqrt{2}$

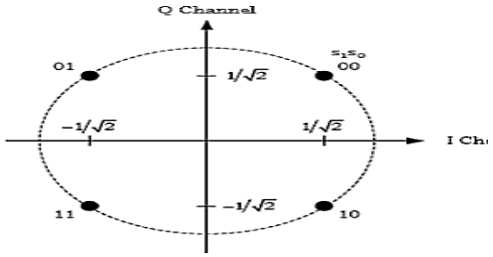

Figure 3 Constellation Mapper

C. FFT AND PIPELINE FFT

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The Fast Fourier Transform (FFT), as an efficient algorithm to compute the Discrete Fourier Transform (DFT), is one of the most important operations in modern digital signal processing and communication systems. The pipeline FFT is a special class of FFT algorithms which can compute the FFT in a sequential manner; it achieves real-time behavior with nonstop processing when data is continually fed through the processor. The primary goal is to optimize pipeline FFT processors to achieve better performance and lower cost than prior art implementations. The R22SDF algorithm architecture shown in Figure (4) has various number of stages as log4N. Every stage contains two butterfly elements, each associated by an Nt feedback shift register. A simple counter creates the control signals. Pipeline registers can be added between butterfly elements and between stages. Registers are also added inside the complex multipliers to reduce the critical path through the summation to the multiplier. The total latency is approximately N + 4 (log4 N – 1) cycles.

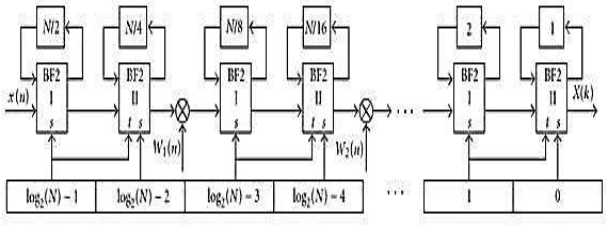

Figure 4 N-point R22SDF pipeline FFT structure

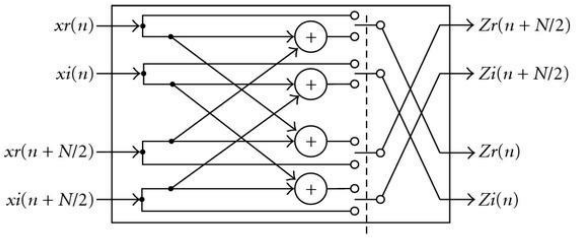

Figure 5 R22SDF BF2 I structure

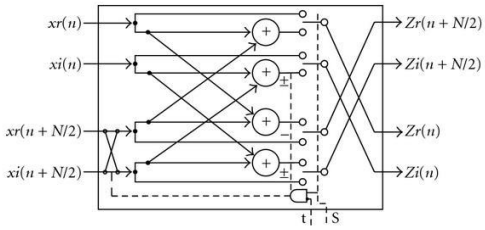

Figure 6 R22SDF BF2 II structure

Radix-22 Single Path Delay Feedback (R22SDF) architecture has two stages in that it consists of 2 to 1 multiplexer in which if the switch is in '0' position the BF2 I structure is said to be in the idle state, and in case if the switch is in '1' position the BF2 II structure is processed and store the values using shift registers, as shown in Figure 5 and 6.

D. PROTOTYPE FILTER

Prototype filters are electronic filter designs that are used as a template to produce a modified filter design for a particular application. They are most often seen in regard to electronic filters and especially linear analogue passive filters. However, in principle the method can be applied to any kind of linear filter or signal processing, including mechanical, acoustic and optical filters Filters are required to operate at many different frequencies, impedances and bandwidths.The utility of a prototype filter comes from the property that all these other filters can be derived from it by applying a scaling factor to the components of the prototype. Most commonly, the prototype filter is expressed as a low pass filter, but other techniques are also possible.

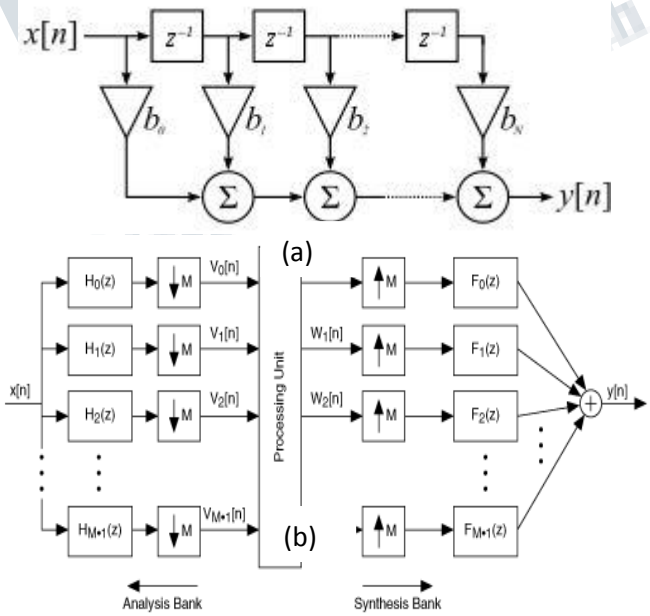

Figure 7 (a) FIR Filter
(b) General Filter bank structure

The above Figure 7 shows the structure of simple FIR filter and the general diagramatic representation of filter bank , which is used at the receiver side to get the better performance of FBMC compared to that of OFDM.

III. RESULTS AND DISCUSSION

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The original data is randomly generated in MATLAB and then the data are given into QPSK modulation. From the QPSK signal, the subcarriers are seperated and then move into IFFT and FFT for better performance are shown below

A.Matlab Simulation:

The below Figure 8 shows the FBMC output simulated in MATLAB.

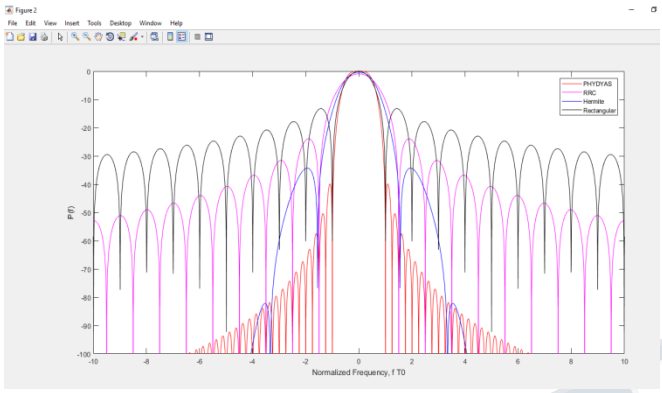


Figure 8 FBMC MATLAB output

B. QPSK Modulation:

The Figure 9 represents the simulated output of QPSK modulator respesctively

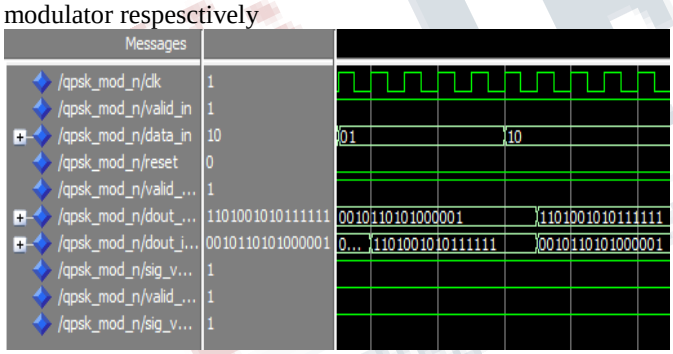


Figure 9 QPSK Simulation output

C. FFT Implementation:

The 8- point FFT with FIR filter is implemented in SPARTAN –6 using Xilinx tool and the Obtained timing summary and device utilization are below:

TIMING SUMMARY:

Minimum period: 7.192ns (Maximum Frequency: 139.039MHz)

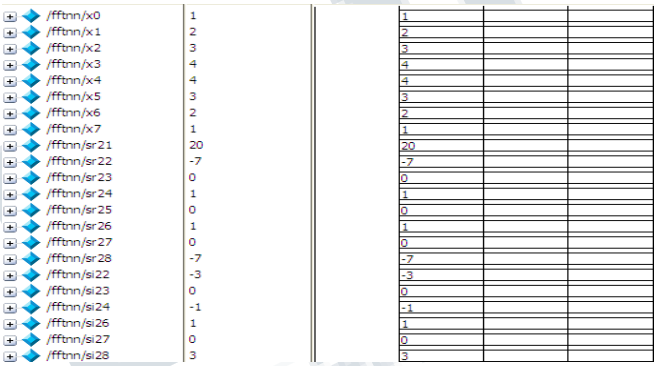
Minimum input arrival time before clock: 6.873ns

Maximum output required time after clock: 9.308ns

DEVICE UTILIZATION:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	2678	18224	14%
Number of Slice LUTs	15191	9112	166%
Number of fully used LUT-FF pairs	2019	15850	12%
Number of bonded IOBs	133	186	71%
Number of Block RAM/FIFO	17	32	53%
Number of BUFG/BUFGCTRLs	1	16	6%
Number of DSP48A1s	32	32	100%

SIMULATION OUTPUT:



D.Pipeline FFT Implementation:

TIMING SUMMARY:

Minimum period: 5.346ns (Maximum Frequency: 187.056MHz)

Minimum input arrival time before clock: 7.123ns

Maximum output required time after clock: 5.693ns

DEVICE UTILIZATION:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	1998	3584	55%
Number of Slice Flip Flops	2137	7168	29%
Number of 4 input LUTs	3072	7168	42%
Number of bonded IOBs	87	173	50%
Number of BRAMs	4	16	25%
Number of MULT18X18s	4	16	25%
Number of GCLKs	1	8	12%

D.Filter Implementation

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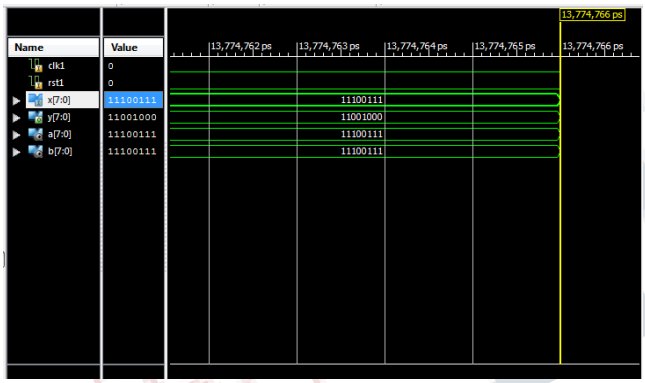
TIMING SUMMARY:
Minimum period: 2.421ns (Maximum Frequency: 413.052MHz)
Minimum input arrival time before clock: 2.440ns
Maximum output required time after clock: 22.738ns.

DEVICE UTILIZATION:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	275	18224	1%
Number of Slice LUTs	401	9112	4%
Number of fully used LUT-FF pairs	238	438	54%
Number of bonded IOBs	19	186	10%
Number of BUFG/BUFGCTRLs	1	16	6%

SIMULATION OUTPUT:



IV. CONCLUSION

The FBMC modulation is done by using MATLAB. The 16–point FFT and the pipeline FFT with prototype filter is implemented in SPARTAN-6 FPGA board. Efficient timing constraints are taken from pipeline FFT than 16-point FFT. From the above results it is clear that the better performance is obtained in pipeline FFT and the prototype filter is applied to get the better performance of FBMC. Hardware requirement of pipelined FFT architecture is compared with FFT of 16-point where, it not only reduce the number of complex multipliers, adders and memory size but also control complexities. The above work can be extended as the pipelined FFT approach for different modulations can be done to improve the transceiver side signal speed in FBMC. Instead of pipelined FFT , we can use parallel FFT (i.e.., replication of pipelined FFT) in the transceiver side to improve the physical layer of FBMC.

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