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A Novel Low-Power Reversible Vedic Multiplier

[1] P.Kiran Kumar, [2] E.Padmaja
Research Scholar in ECE, KL University
Asst. Professor in ECE, Balaji Institute of Technology and Science

***Abstract* - In reversible computing, modelling low-power circuits is one of the most important techniques. As a result of its wide range of applications, major works have been proposed in realizing reversible circuits including primary reversible gates and adders. In reversible computation, multiplier circuits play a vital role in practical applications like quantum dot cellular automata, DNA computing, nanotechnology and low-power CMOS designs. Hence superior multiplier architectures are bound to increase the efficiency of the system. The Vedic multiplier is one such optimistic solution. Implementing this with reversible logic further decreases power dissipation. In this paper, a novel reversible Vedic multiplier is proposed by making use of an algorithm or sutra called Urdhva Tiryagbhyam meaning vertical & crosswise. The power dissipation of proposed reversible multiplier design is reduced by 72.47 %. The reduction in power dissipation is highly achieved by reducing the number of gates which comprise reduction of 12.5 %. The constant inputs are reduced by 16.5 % and a reduction of 28 % is obtained in garbage outputs.**

Keywords: Reversible computation, nanotechnology, DNA computing, Urdhva Tiryagbhyam, vedic multiplier.

INTRODUCTION

Importance of Low-energy computing is increasing with increase in power dissipation. Low-energy is very important in computers where performance is not demanding but life of battery is primary interest. Reversible computing is one such an important approach in this aspect. The input bits are vanished when a digital block produce output bits in conventional computers. This process is irreversible and thus the computation made in conventional computers is also irreversible. In digital logic computation, every bit of information vanished, dissipates KTln2 Joules [1] of heat energy where T is temperature of performing computation, K is Boltzmann's constant. If a computation is executed in reversible way then KTln2 Joules of energy dissipation will not take place. This is because during execution there is a direct communication between energy dissipation and number of bits erased. Dissipation less circuit should be lossless circuit theoretically. But this is not practically possible. Parker et al. [3] , showed that even when information is moved at the time of computation heat dissipation takes place. An operation is called reversible if there is neither entropy change nor conversion of energy to heat. The computational state just before an operation is uniquely found out by its state just after operation i.e., information about state of computation is not lost. Thus, the systems designed by reversible logic are absolute state machines [4]. The outputs are combinations of numbers 0 to (2n 1) in an n-output reversible gate. In reversible gate the outputs are 1's for half the number of inputs. Thus reversible gates are balanced. Balanced functions are implemented by circuits consisting of reversible gates. No balanced functions can be implemented with reversible gates along with constant inputs and garbage outputs. Reversible circuits are able to function both in forward (input ! output) and backward direction (input output) simply by physically choosing direction of calculation [5]. However synthesis of these networks differs from conventional boolean gates. Two constraints are added for reversible network synthesis, namely feedback and fan-out are not accepted [6]. Thus cascading reversible gates is the only feasible approach. A reversible gate by interpretation is an n-input n-output (as shown in Fig.1) cell with one-to-one mapping between inputs and outputs.

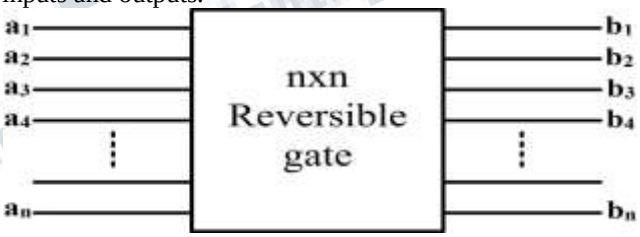

Fig. 1. n x n Reversible gate

From Fig.1, a_1, a_2, a_3,.....,and are n-inputs and b1, b2, b3,.....,bn are n-outputs.

Any reversible function is a bijective function. Physical reversibility and logical reversibility should be satisfied by every reversible gate. Unique output for unique input (h0; $1i^n$! h0; $1i^n$) is the property of logical reversibility. If a gate is reversible logically then it is also reversible thermodynamically. Some important properties are to be considered in designing reversible circuits which are as follows: The count of inputs should be equal to the count of outputs. n n circuit have n! Combinations of data are at output. For illustration, if inputs are 4+7+2 then the outputs may be one of 2+7+4, 2+4+7, 7+2+4, 7+4+2, 4+2+7 and 4+7+2. Therefore no data is destroyed or added during operation [4]. It obeys the second law of thermodynamics.

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Multiplier circuits originally have two units. i) Partial product generator and ii) Multi-operand addition circuit. The partial product generation circuit is same for both signed and unsigned multiplication. The partial product generates product terms that are to be added to carry out multiplier operation. Some basic terms oftenly used in reversible logic are listed as:

A. Constant input

These are the control inputs that are maintained at either logic-0 or logic-1 to integrate the given logic function.

B. Garbage Output

The unused/unwanted outputs in reversible logic synthesis are garbage outputs. These garbage outputs cannot be avoided as they are required to maintain reversibility.

Inputs + Constant inputs = Outputs + Garbage outputs

C. Quantum Cost

The number of 1 1 and 2 2 quantum gates required in realizing a reversible gate is called Quantum cost. Decreasing the quantum cost of a digital circuit is always problematic. The quantum cost of some basic reversible gates is: Feynman-1, Toffoli-5, Fredkin-5 and Peres-4.

The rest of the paper is organized as follows. Section II describes Basic reversible gates that are used in this paper. Importance of Vedic multiplication algorithm is explained in Section III. Existing architectures of different reversible multipliers are discussed in Section IV. The process of Vedic multiplication, line diagram of Urdhva Tiryagbhyam algorithm and proposed low-power Vedic multiplier are explained in Section V. The different performance parameters of existing and proposed multipliers are summarized in Section VI.

II. BASIC REVERSIBLE GATES

Over the years, several reversible gates are proposed. E.g. Feynman [7], Toffoli [8], Fredkin [9], Peres [10].

A. Feynman Gate

Feynman gate is 2-input 2-output reversible gate (Fig.2). It is also called as CNOT gate because one of the inputs can be used either to invert or to pass as it is. Mostly feynman gate is used in situations where fan-out is needed. Thus Feynman gate is also called as fan-out gate.

F EY NMAN : (((X; Y) (A; B)); ((0; 1; 3; 2) (0; 1; 2; 3))) [11]

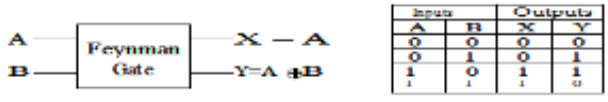
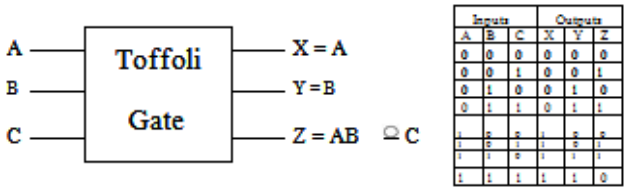


Fig. 2. Feynman gate

B. Toffoli Gate

Toffoli (TG) gate is 3-input 3-output gate (Fig.3). It is also called as CCNOT gate because of its operation. For a general toffoli gate with n-input and n-output, the operation is expalined as follows. All inputs from 1 to (n-1) are passed as it is to output in toffoli gate. 1 to (n-1) inputs controls the nth output. The nth input is inverted at output if all the inputs from 1 to (n-1) are made 1's, else original signal is passed. From Fig.3, A and B are passed as it is to the first two outputs. To invert third input C, we use A and B as controlling inputs. Thus toffoli gate is called as controlled controlled NOT gate. Toffoli gate is universally primitive because there is only one recurring relation between 101 and 110. This property is also satisfied by feynman and fredkin gates [12].

T OF F OLI : (((X; Y; Z) (A; B; C)); ((0; 1; 2; 3; 4; 5; 7; 6) (0; 1; 2; 3; 4; 5; 6; 7)))



C. Peres Gate

Peres gate (Fig.4) is also known as modified toffoli gate because it contains toffoli and feynman gate. Peres gate is preferred over toffoli gate because of its reduced quantum cost. Peres gate is not universally primitive because there are no recurring relations between any of the input combinations.

P ERES : (((X; Y; Z) (A; B; C)); ((0; 1; 2; 3; 6; 7; 5; 4) (0; 1; 2; 3; 4; 5; 6; 7)))

Fig. 4. Peres gate

III. VEDIC MULTIPLICATION

The word Vedic is derived from the word veda, which means the store house of all knowledge [13]. Vedic mathematics is mainly based on 16 sutras dealing with various branches of maths like algebra, arithmetic, geometry etc. Vedic mathematics is not only a mathematical wonder but also it is logical. Vedic mathematics reduces the cumbersome calculations in conventional mathematics to a very simple calculation. This is because, the Vedic sutras are claimed to be based on the natural principles on which the human mind works. In Vedic multiplication, two sutras are dedicated to multi-plication. One is Nikhilam Navatashcaramam Dashatah sutra and the other is Urdhva Tiryagbhyam sutra. In this paper we focus on Urdhva Tiryagbhyam sutra.

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Vedic multiplier is based on Vedic multiplication sutras. These sutras have been traditionally used for the multiplication of two numbers in the decimal number system. The same idea can be applied to the binary number system to make algorithm compatible with the digital hardware.

IV. EXISTING ARCHITECTURES

In the recent years many reversible circuits are proposed as a replacement for conventional irreversible circuits. On the other hand, because of the substantial use of multipliers in computer systems, various reversible circuits for implementing multipliers have been proposed. Haghparast et al. [14], have proposed a reversible multiplier circuit which consists of two parts. The first part is partial product generation circuit and the second part takes the result from first part, performs addition for producing the final result (i.e. four operand addition circuits). The design uses array of Peres gate for partial generation circuit and then additional adder circuit consists of Peres gate and HNG gates. Another study in reversible multiplier design has been proposed by Bhagyalaxmi and Venkatesha [15], it consists of a fan-out generation circuit, partial product generation circuit and four operand addition circuit to form a 4 4 multiplier. This proposed design is a combination of BVF gates, carry save adder and carry propagating adder for producing the final results. Other similar designs have been proposed in [16]. The only difference is the type of gate used in the design. This design consists of peres gate, carry save adder and carry select adder. In [17], Anindita Banerjee used TSG, PFAG, and HNG in their architecture. A total of 56 different gates used in this multiplier. Hatkar et al. in [18], used TG, HNG, PG gate. 42 gates are used in which there are 52 garbage outputs and 42 constant inputs.

V. PROPOSED WORK

The proposed multiplier is based on the algorithm Urdhva Tiryagbhyam (Vertical & crosswise) of Vedic mathematics. It literally means Vertically & Crosswise. It is based on novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryagbhyam algorithm.

A. Urdhva Tiryagbhyam algorithm for 4 4 multiplier

To elucidate the multiplication algorithm using Urd-hva Tiryagbhyam algorithm, two binary numbers a3a2a1a0, b3b2b1b0 are considered.

Multiplicand							a3	a2	a1	a0
Multiplier							b3	b2	b1	b0
	H	G	F	E	D	C	B	A
	S7	S6	S5	S4	S3	S2	S1	S0

From the multiplication in algorithm, S0, S1, S2,....., S7 are the final products of the multiplication. The intermediate multiplication process is explained in Parallel Computaion Methodology. Where CP represents Cross Product (Vertically & Crosswise)

1)	CP	a0 b0	A=a0b0
2)	CP	a1 a0 b1 b0	B=a2b0+a0b2+a1b1
3)	CP	a2 a1 a0 b2 b1 b0	C=a2b2+a0b2+a1b1
4)	CP	a3 a2 a1 a0 b3 b2 b1 b0	D=a3b0+a0b3+a1b2+a2b1
5)	CP	a3 a2 a1 b3 b2 b1	E=a3b1+a1b3+a2b2
6)	CP	a3 a2 b3 b2	F=a3b2+a2b3
7)	CP	a3 b3	G=a3b3

B. Analysis of Urdhva Tiryagbhyam using Line diagram

Line diagram for multiplication of two 4 bit numbers is shown in Fig.7. For the purpose of understanding each bit of multiplicand and multiplier is represented by a circle. Least significant bit S0 is obtained by multiplying least significant bits of multiplicand and multiplier. Initially, least significant bits are multiplied, which gives least significant bit of product (vertical). Then least significant bit of multiplicand is multi-plied with the next higher bit of the multiplier and added with the product of least significant bit of multiplier and succeeding higher bit of multiplicand (Crosswise). The sum gives second bit of product and carry is added to the output of next stage sum, obtained by the crosswise and vertical multiplication and addition of 3 bits of the 2 numbers from least significant position. After all the 4 bits are processed with crosswise multiplications and addition gives the sum and carry. The sum is corresponding bit of the product and carry is again added to the succeeding stage multiplication and addition of 3 bits except least significant bit. The same operation continues until the multiplication of the two most significant bits of multiplicand and multiplier to give most significant bit of the product.

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C. Proposed Low-Power Vedic Multiplier

The design of 4 4 proposed novel vedic multiplier is done using two steps Partial Product Generation Multi Operand Addition

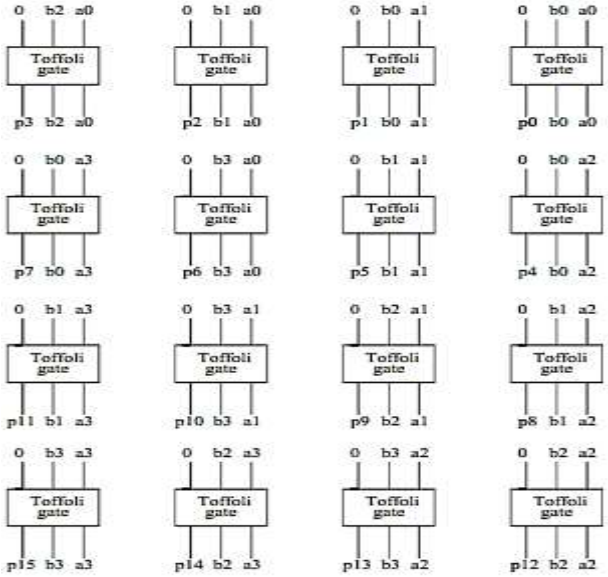

Fig. 5. Circuit for generating partial product

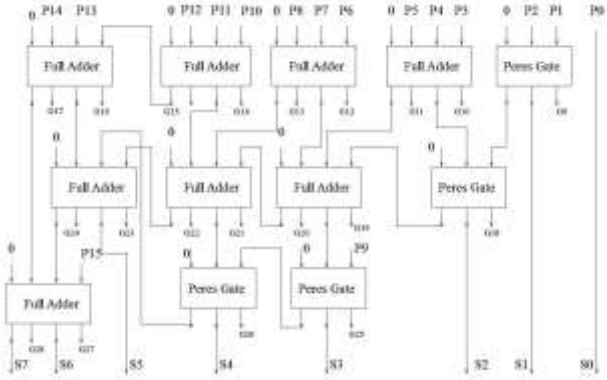

Fig. 6. Multi Operand addition circuit

TABLE I

PERFORMANCE ANALYSIS OF DIFFERENT MULTIPLIERS

Gates Used	Multiplier Type	Number Of Gates Used	Garbage Output	Constant Input	Power (mW)	Quantum Cost	Delay (ns)
TSG,PFAG,HNG	[17]	56	34	40	8.37	144	117.1
PG,HNG	[14]	52	52	52	7.01	152	115.2
PG,BVF,DPG	[15]	40	52	52	6.81	152	113.5
TG,PG,HNG	[18]	45	46	46	5.67	152	101.5
PG,FA,HA	[16]	42	52	42	4.36	152	94.9
TG,PG,FA	Proposed	35	33	35	1.20	108	12.8

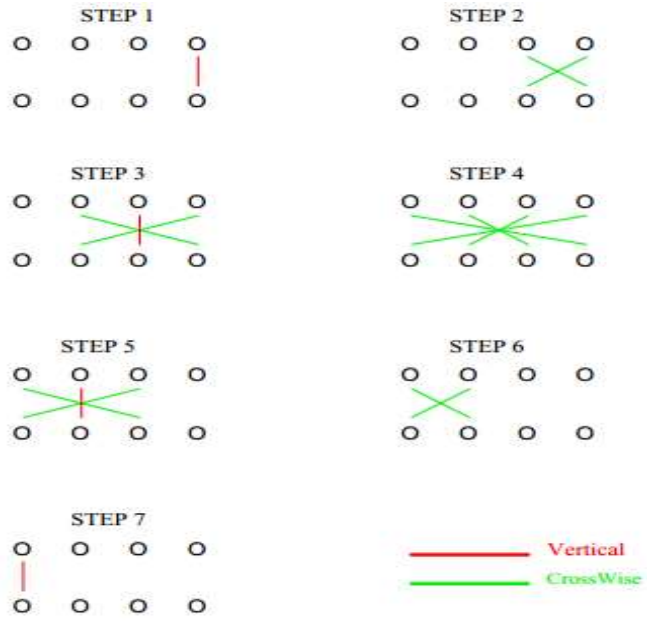

Fig. 7. Urdhva Tiryagbhyam algorithm analysis using line diagram

Partial Product Generation: Partial products of pro-posed 4 4 Vedic multiplier requires 4 4 = 16 two input AND operations. These AND operations are realized by toffoli gates by making its third input C as logic-0 (C=0). It is a better circuit as it has less hardware complexity and low quantum cost contrast to other existing partial product generation circuit. Every single TG gate with inputs A, B, C and with constant value of logical-0 in its third input (i.e C) generates 3 outputs which are X=A, Y=B, Z=AB. The last output (Z=AB) is used for generation of partial products. The number of AND operations needed are 4 4 = 16. Therefore same number of TG gates is required for partial product generation as shown in Fig.5. Multi Operand Addition: After generating the partial products, we have to add the bits of each column given in Fig.6. For the addition these bits, we have used FA and HA. We have to add these bits in such a way that our circuit gives the best outcome with minimum power. Our proposed multi operand addition circuit shows the way of adding the bits and this proposed circuit consists of minimum number of garbage outputs, constant inputs and quantum cost. In this proposed Vedic multiplier, HA is realized by peer's gate by making its third input as logic-0. An optimum power dissipation Full Adder is proposed in [19] with minimum constant inputs, garbage outputs and quantum cost is used in proposed Vedic multiplier design.

The proposed Vedic multiplier is implemented in Cadence

Virtuoso Schematic editor in 180 nm technology and found suitable results. It shows the better performance than the existing multiplier architectures [17], [14], [15], [18], [16].

VI. CONCLUSION

A novel low-power reversible Vedic multiplier is proposed in this paper. It is compared with existing reversible multi-plier architectures in terms of garbage output, constant inputs, quantum cost, power and delay. The proposed Vedic multiplier shows reduction of number of gates by 12.5%, constant inputs by 16.5%, garbage output by 28%. The remarkable appreciation of proposed Vedic multiplier is reduced power dissipation which accounts to 72.47% than multipliers that are existed.

REFERENCES

[1] R. Landauer, "Irreversibility and heat generation in the computing process," IBM Journal of Research and Development, vol. 5, no. 3, pp. 183–191, July 1961.

[2] C. Bennett, "Logical reversibility of computation," IBM Journal of Research and Development, vol. 17, no. 6, pp. 525–532, Nov 1973.

[3] M. C. Parker and S. D. Walker, "Is computation reversible?" Optics communications, vol. 271, no. 1, pp. 274–277, 2007.

[4] T. Chattopadhyay, "Optical logic circuits using double controlled logic gate," Optoelectronics, IET, vol. 7, no. 5, pp. 99–109, October 2013.

[5] S. Burignat, M. K. Thomsen, M. Klimczak, M. Olczak, and A. De Vos, "Interfacing reversible pass-transistor cmos chips with conventional restoring cmos circuits," in Reversible Computation. Springer, 2012, pp. 112–122.

[6] P. Gupta, A. Agrawal, and N. Jha, "An algorithm for synthesis of reversible logic circuits," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, vol. 25, no. 11, pp. 2317–2330, Nov 2006.

[7] R. Feynman, "Quantum mechanical computers," Foundations of Physics, vol. 16, no. 6, pp. 507–531, 1986.

[8] T. Toffoli, "Reversible computing," in Automata, Languages and Pro-gramming, ser. Lecture Notes in Computer Science, J. de Bakker and J. van Leeuwen, Eds. Springer Berlin Heidelberg, 1980, vol. 85, pp. 632–644.

[9] E. Fredkin and T. Toffoli, "Conservative logic," International Journal of Theoretical Physics, vol. 21, no. 3-4, pp. 219–253, 1982.

[10] A. Sarker, A. N. Bahar, P. K. Biswas, and M. Morshed, "A novel presentation of peres gate (pg) in quantum-dot cellular automata (qca)," European Scientific Journal, vol. 10, no. 21, 2014.

[11] S. Mahammad and K. Veezhinathan, "Constructing online testable circuits using reversible logic," Instrumentation and Measurement, IEEE Transactions on, vol. 59, no. 1, pp. 101–109, Jan 2010.

[12] M. Morrison and N. Ranganathan, "Synthesis of dual-rail adiabatic logic for low power security applications," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, vol. 33, no. 7, pp. 975–988, July 2014.

[13] Jagadguru Swami Sri Bharathi Krishna Tirthji Maharaja, "Vedic math-ematics," 1986.

[14] M. Haghparast, S. Jassabi, K. Navi, and O. Hashemipour, "Design of a novel reversible multiplier circuit using hng gate in nanotechnology," in World Applied Science Journal, 2008. IEEE, 2008, pp. 974–978.

[15] H. Bhagyalakshmi and O. Venkatesha, MK, "An improved design of a multiplier using reversible logic gates," in International Journal of Engineering Science and Technology, 2010. IJEST, 2010, pp. 3838– 3845.

[16] F. Naderpour and A. Vafaei, "Reversible multipliers: decreasing the depth of the circuit," in Electrical and Computer Engineering, 2008. ICECE 2008. International Conference on. IEEE, 2008, pp. 306–310.

[17] A. Banerjee and A. Pathak, "An analysis of reversible multiplier cir-cuits," arXiv preprint arXiv:0907.3357, 2009.

[18] A. Hatkar, A. Hatkar, and N. Narkhede, "Asic design of reversible mul-tiplier circuit," in Electronic Systems, Signal Processing and Computing Technologies (ICESC), 2014 International Conference on. IEEE, 2014, pp. 47–52.

[19] Y. Van Rentergem and A. De Vos, "Optimal design of a reversible full adder," International Journal of Unconventional Computing, vol. 1, no. 4, p. 339, 2005.