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# Implementation of Logic Circuits with Low Energy Charge Recovery Logic

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***Abstract* - Various energy recovery circuits have been proposed for reducing the power dissipation in CMOS logic circuits. This paper presents three Logic Circuits implemented using charge recovery logic. They are completely unique boost logic known as pseudo-NMOS boost logic (PNBL), to get low energy consumption and efficient-speed as compare to CMOS binary logic. PNBL is faster and compact charge recovery logic and it related to boost logic family. These logic circuits have less operating energy dissipation due to charge recovery logic. To exhibit the performance of Logic circuits are implemented with PNBL and compared with CMOS in 180nm technology. Simulation results show that logic circuits with PNBL recover the charge 57.14nJ at the frequency of 1GHZ that is approximately 105 times conserve energy as compared to conventional CMOS technology. Charge recovery logic also has one more advantage that it provided complemented and non-complemented both output at a time with small area trade-off.**

**Index Terms: Pseudo N-MOS Boost Logic, Low Energy Consumption, Charge recovery logic, Adiabatic Logic.**

## I. INTRODUCTION

Today scenario in VLSI design energy dissipation is one of the most prominent issues. Energy dissipation may be essential factor because of the disability to get back the power from the circuit. Charge recovery logic can get back the energy from the circuit so this technique is used because of its energy conservation. [1]

In many literatures the Charge recovery logic represented smart work over low energy as a result of circuit energy is preserved rather than consumption as heat. But the one trade-off is finding between power dissipation and performance. [2]

Variety of things such as threshold voltage and transition rate will have an effect on the energy efficiency of charge recovery logic, so this factor can affect the performance of the circuitry. But boost logic operates with less energy consumption as compare to $CV^2/2$ that is the usual energy consumption of CMOS based circuit [3].

Charge recovery logic's in ref. [4] toughly work correctly only when the operating frequency of these circuits increases. Charge recovery logic uses two phase logic that consists of energy recovery stages with conventional switches which can achieve significant energy. [5]

For boost logic, when the power clock is lesser a waiting status exists, the circuits are idle for half cycle of power clock so that the operation performance is not allowed. Fig. 1 shows the working principle of boost logic family. [6]

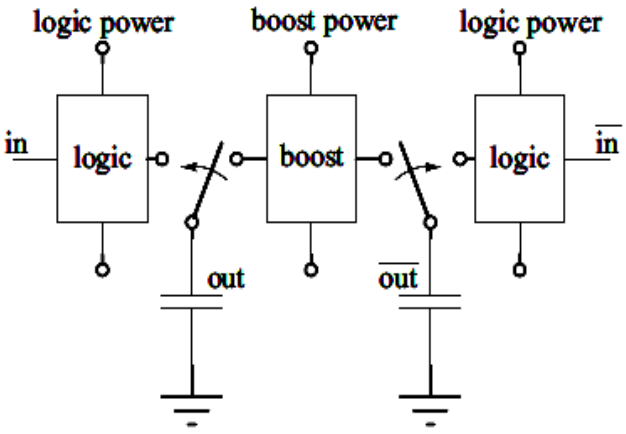


***Fig.1. Boost logic family basic operation***

In first step logic values measures within the logic block and in second step this logic value boosted to higher voltage using the boost block. Boost logic is used in synchronous sequential circuits so this structure can be divided into two parts so boost logic will operated by power clock. In this research paper, charge recovery logic referred to as PNBL designed. Boost logic's PNBL technique is highly drivable as compare to other logics. For certify the effect of PNBL in decreasing energy consumption of logic circuits compared to conventional CMOS logic circuits with the more area trade off. [7]

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## II. PSEUDO NMOS BOOST LOGIC

In this research paper, operations of Pseudo- NMOS Boost Logic are implemented. In these circuits without overlapping intervals clock and clock bar are used so DC power is not used in PNBL. In PNBL circuits PUNs in each rail are replaced with one PMOS transistor and gates are connected with clock of the PMOS transistors. PNBL uses less number of transistors so that the input capacitances of PNBL are smaller. In the sequential circuits; the input capacitance of one gate is the load capacitance of another PNBL gates so the major power consumption is due to load capacitance in PNBL circuits. Clock is in high voltage whereas clock bar is in lower voltage in the analysis stage. When clock bar is low, PMOS PM0 and PM2 behave as Pull-Up Network and makes pull up network always on, and therefore the complementary inputs make one Pull down network and makes pull down network always on. In pseudo-NMOS circuits same methodology is used. In Pseudo Boost logic (PBL) threshold voltage loss does not exists because PMOS transistor uses for pull up the logic is in always high state. [8]

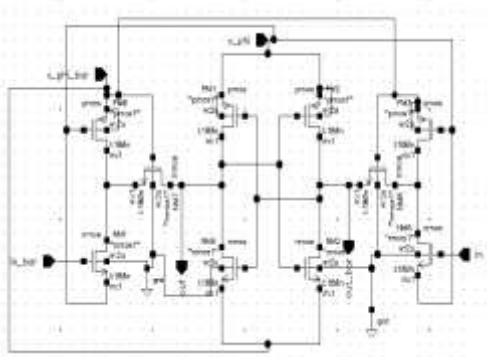

*Fig.2. Structure of PNBL*

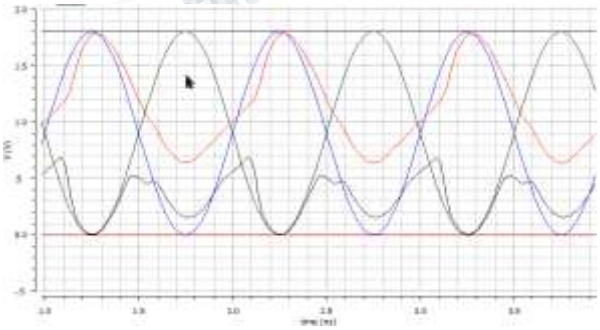

*Fig.3. Output Waveform of PNBL*

In the operation of Pseudo NMOS Boost logic (PNBL) throughout this operation, pass gates NM7 and NM8 will be on since clock is high. Voltage created by the charge recovery block will hardly affect these values, in the analysis stage. In the charge recovery stage, clock bar will be in low half cycle whereas clock will be in high half cycle. Pass gates NM7 and NM8 are each off when the clock bar is low.

Initially Input 'in' is high and 'in_bar' is low so the NM1 becomes off and NM5 becomes on. V_phi is low so PM3 and PM5 are on and at the same time V_phi_bar is high so NM7 and NM8 are on. So the Out is initially high and Out_bar is initially high but it becomes high to low through the path of NM8 to NM5. So that we have been achieved the boosted out and out_bar both in the same time. This operation vice versa is also true.

Fig. 4 shows the buffer series of PNBL and Fig.5 shows the output wave of PNBL gates buffer1 and buffer2. In this circuit output of first stage is the input of second stage. Each buffer internal operation is same as previously explained circuit of PNBL.

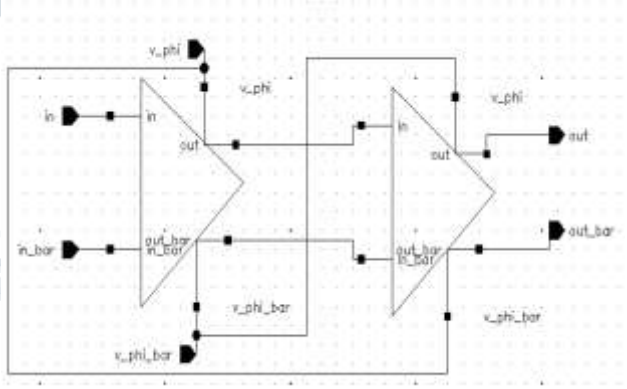


*Fig.4. Buffer series of PNBL*

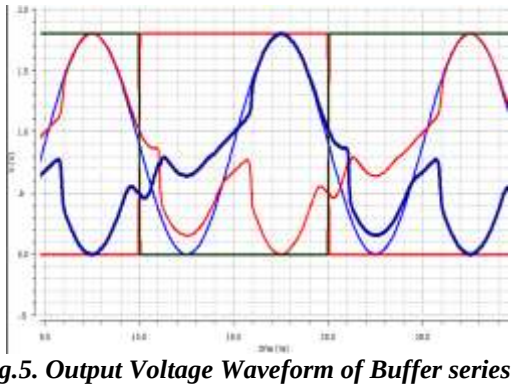

*Fig.5. Output Voltage Waveform of Buffer series of PNBL*

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## III. IMPLEMENTATION OF DIFFERENT LOGIC CIRCUIT OF PNBL

5-bit comparator schematic using PNBL is shown in Fig.6.
In this schematic upper part shows the boost circuit and below left part shows the Pull up network and right part shows the pull down network of the 5-bit comparator circuit. Interesting fact is for both pull up and pull down network NMOS transistor is used. Because in PNBL circuits boost block circuit act as pull up network and logic circuit act as pull down network.

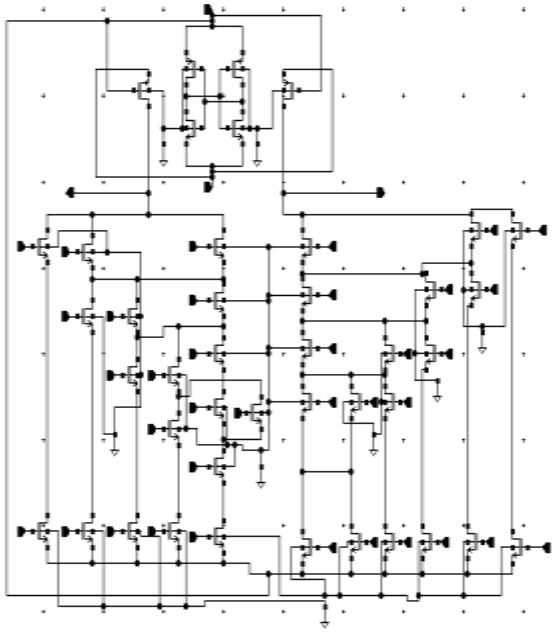

*Fig.6. 5-bit comparator schematic*

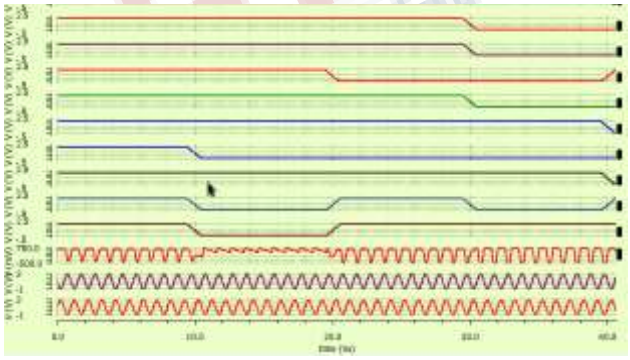

*Fig.7. Output Waveform of 5-bit comparator schematic*

Schematic of 4-bit PNBL multiplexer is shown below in Fig.8. In this circuit pull up network and pull down network shows out and out bar respectively. So it can drive more than one function at a time.

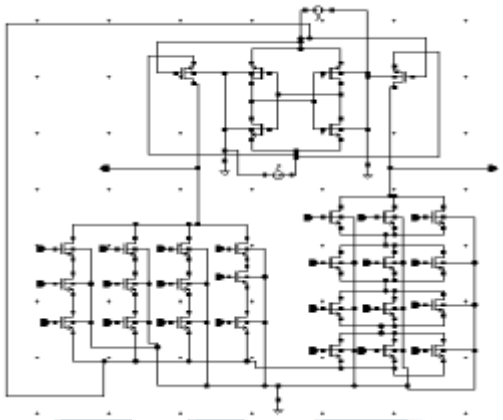

*Fig.8. 4- bit Multiplexer with PNBL*

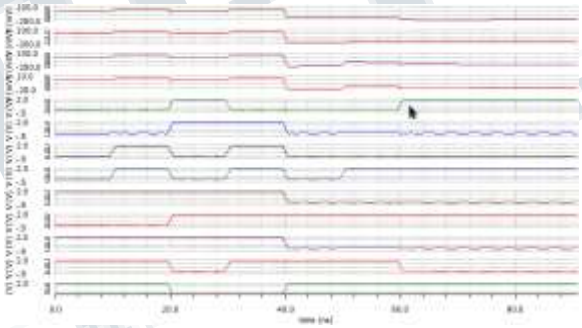

*Fig.9. Output Waveform of 4- bit Multiplexer with PNBL*

Following schematic shows the Edge triggered D Flip-flop with PNBL. This provides the more functionality with less power dissipation with small area trade off as compare to conventional static CMOS technology.

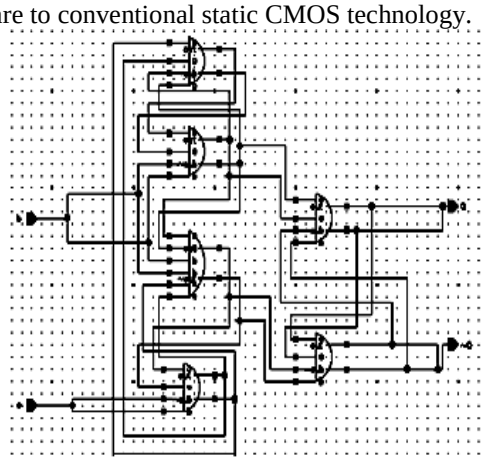

*Fig.10. Edge Triggered D-flip flop with PNBL*

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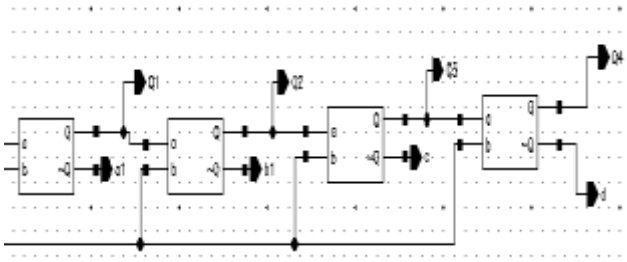


*Fig.11. 4-bit Accumulator Register with PNBL*

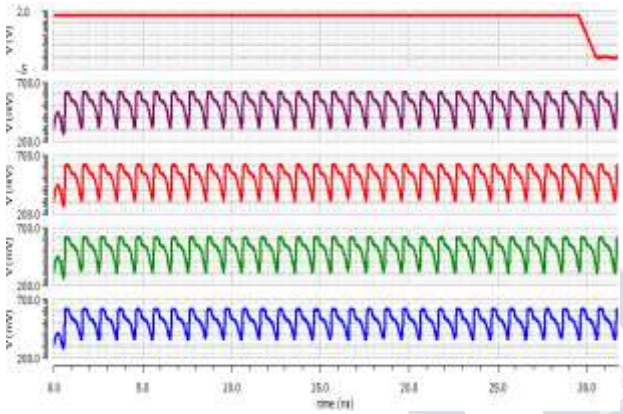


*Fig.12. Output Waveform of 4-bit Accumulator Register with PNBL*

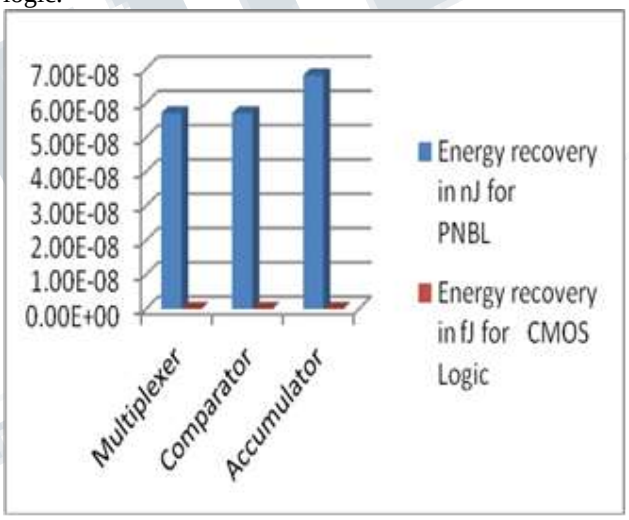
## IV. SIMULATION RESULTS AND DISCUSSION

Compare the energy recovery against the pseudo NMOS boost logic represented by Multiplexer, Comparator and Accumulator register. Energy recovery of different logic circuit is given below

### *I. Energy recovery of different logic circuits with PNBL compared with CMOS logic circuits*

| Name of the logic circuit | Energy recovery in nJ for PNBL | Energy recovery in fJ for CMOS Logic |
|---|---|---|
| Multiplexer | -57.14 | -703.3 |
| Comparator | -57.14 | -709.1 |
| Accumulator | -68.12 | -706.4 |

All the values are negative that means it shows the energy recovery not the energy dissipation. Energy recovery of pseudo NMOS Boost Logic based Multiplexer; Comparator and Accumulator register is much more compare to the energy recovery of the conventional CMOS based logic. Charge recovery of conventional CMOS Logic is approximately negligible. This energy recovery is approximately 105 times more with high speed with trade off. Numbers of used transistors are more in PNBL based logic circuits compared to the conventional CMOS based logic circuits. Because in the PNBL implemented one extra Boost logic circuit in place of PMOS which reduces the number of transistors but for Boost Logic circuit we needed complementary and non complementary circuit so that number of transistors we needed more compare to the conventional CMOS based logic.




### *II. Area consumption of logic circuits with PNBL compared with CMOS logic circuits.*

| Name of the Logic circuit | Total Number used of Transistors used for PNBL | Total Number of Transistors used for CMOS Logic |
|---|---|---|
| Multiplexer | 42 | 72 |
| Comparator | 42 | 36 |
| Accumulator | 248 | 184 |

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## CONCLUSION

In this paper pseudo NMOS Boost logic based Logic circuits are proposed. Comparing with conventional CMOS based Logic circuits. The projected PNBL based logic circuits conserve approximately 81250 times energy compared to the conventional CMOS based logic circuits with small area trade off.

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