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Performance Analysis of Vedic Multiplier Based on Various Adders

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Abstract: **- Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. This paper proposes the design and implementation of 16 Bit Vedic Multiplier based on carry save adder using the techniques of Ancient Indian Vedic Mathematics. The proposed Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using Xilinx ISE 14.1 design suite. The design is synthesized using Artix-7 FPGA family. The Artix-7 family is based on 28nm design which operates at 50% lower power than 45 nm technology. In this paper peak memory usage, delay, power, power-delay product and energy-delay product are the parameters taken for comparison. The results that were taken for comparison has previously done for 16 bit Vedic multiplier based on 16 bit modified carry select adder, 16 bit ripple carry adder and 16 bit kogge-stone adder[2] and here that results were constituted in this paper for comparative study with 16 bit Vedic multiplier based on carry save adder for same parameters. This paper also gives information of Urdhva Tiryakbhyam algorithm of Vedic Mathematics which is utilized for multiplication to improve the speed and area of multipliers. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros and scaled to higher bit levels. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased.**

Keywords: - Vedic Multiplier, VHDL, Urdhva Tiryakbhyam, Modified carry select adder, Vedic multiplier, Ripple carry adder, Kogge stone adder, Carry save adder

I. INTRODUCTION

Vedic mathematics is the name given to the ancient system of mathematics, or, to be precise, a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved – be it arithmetic, algebra, geometry or trigonometry.Conventional mathematics is an integral part of engineering education since most engineering system designs are based on various mathematical approaches. The need for faster processing speed is continuously driving major improvements in processor technologies, as well as the search for new algorithms. A multiplier is one of the key hardware blocks in most digital signal processing systems. With advances in technology, many researchers have tried to design multipliers which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. The Vedic mathematics approach is totally different and considered very close to the way a human mind works. In this work, we try to present multiplication operations and the implementation of these using Vedic mathematical methods in VHDL language.

II. VEDIC MATHEMATICS

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upasutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful. The word "Vedic" is derived from the word "Veda" which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or

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aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically.
(Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
1. Chalana-Kalanabyham – Differences and Similarities.
2. Ekadhikina Purvena – By one more than the previous One.
3. Ekanyunena Purvena – By one less than the previous one.
4. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
5. Gunita samuchyah – The product of the sum is equal to the sum of the product.
6. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
7. Paraavartya Yojayet – Transpose and adjust.
8. Puranapuranabyham – By the completion or non-completion.
9. Sankalana- vyavakalanabhyam – By addition and by subtraction.
10. Shesanyankena Charamena – The remainders by the last digit.
11. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
12. Sopaantya dvayamantyam – The ultimate and twice the penultimate.
13. Urdhva-tiryagbhyam – Vertically and crosswise.
14. Vyashtisamanstih – Part and Whole.
15. Yaavadunam – Whatever the extent of its Deficiency.

Multiplication of two decimal numbers using Urdhva Triyakbhyam Sutra

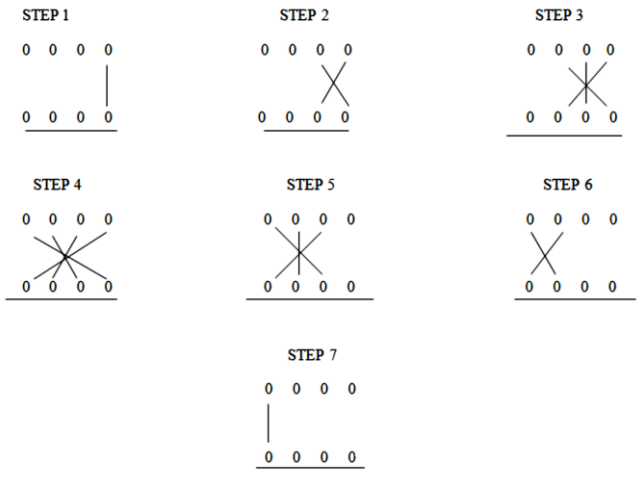

Fig 1: Line diagram for multiplication of two 4 – bit numbers

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general Mathematical formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. Fig [1] shows the concept of multiplication for Urdhva Tiryakbhyam of 4-bit number using line diagram. It is time, space and power efficient. “Urdhva Tiryakbhyam” (Vertical and Crosswise) sutra (Algorithm) is a general multiplication formula equally applicable to all cases of multiplication. The algorithm generates all partial product and sum in one step. To illustrate multiplication operation, consider fig [2] which Shows two decimal number multiplies i.e. 234 * 159.

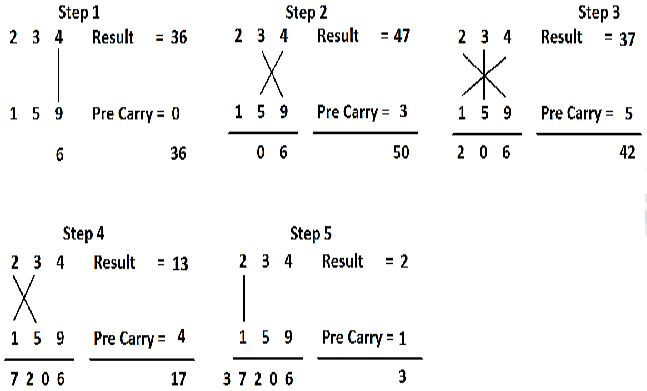

Fig 2: Multiplication using Urdhva Tiryakbhyam

The algorithm is generalized for NXN bit number .This Multiplier has advantage that when we increase the number of bits ,gate delay and area increases very slowly compared to other multipliers. Due to its regular structure, Multiplier processing power increase by increasing the input and output data bus widths.

III. ADDERS FOR COMPARISON

Ripple carry adder
Modified carry select adder
Kogge stone adder
Carry save adder

RIPPLE CARRY ADDER:
The ripple carry adder is constructed by cascading full adders blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. The block diagram of 4-bit carry adder in Fig [3].A number of full adders may be added to the ripple carry adder or ripple carry adders of different sizes may be cascaded in order to accommodate binary vector strings of

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larger sizes. For an n-bit parallel adder, it requires n computational elements.

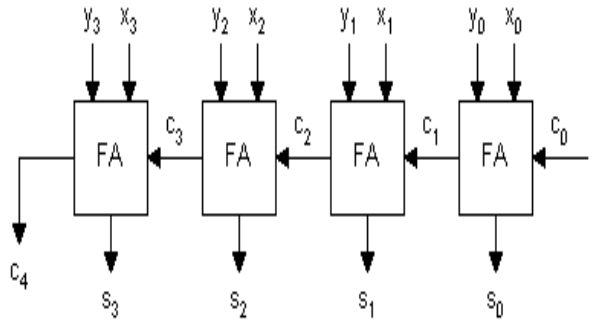

Fig 3: Block diagram of 4- bit ripple carry adder

Modified carry select adder:

The modified carry select adder is used as an alternative of the ripple carry adder. Using Binary to Excess-1 Converter instead of Ripple Carry Adder in the regular Carry Select Adder we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder structure. The performance of the modified carry select adder is better as compared to the ripple carry adder and the kogge stone adder.4-bit Binary to Excess-1 Converter, used for designing the modified carry select adder is shown in Fig[4]

The Boolean expressions of the 4-bit BEC are (note the functional symbols ~ NOT, & AND, ^XOR):

X0 = ~B0 (1)
X1 = B0^B1 (2)
X2 = B2^ (B0 & B1) (3)
X3 = B3^ (B0 & B1 & B2) (4)

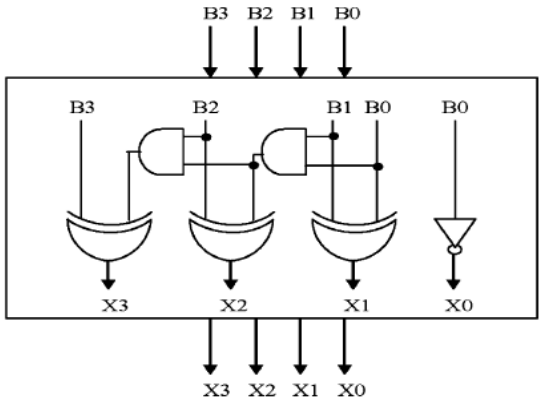

Fig 4: 4-bit Binary to Excess-1 Converter, used for designing the modified carry select adder [3]

Kogge stone Adder:

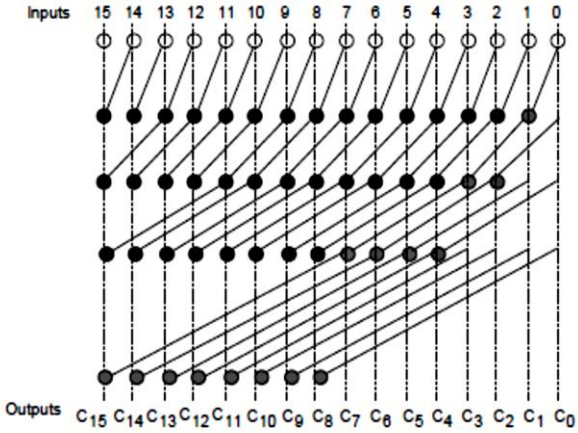

Fig 5: Prefix Graph of a 16-bit Kogge-Stone Adder

The Kogge-Stone Adder was first developed by Peter M. Kogge and Harold S. Stone in 1973. Kogge-stone adder is a parallel prefix formation of Carry Look-ahead Adder. It can be shown as a parallel prefix adder consisting of carry operator nodes.

Kogge-Stone structure is very attractive for high-speed applications. The delay of the structure is given by log2n.This structure possesses [(n)(log2n)-n+1] computation nodes where n is the number of bits. Prefix Graph of a 16-bit Kogge-Stone Adder is shown in Fig [5].

CARRY SAVE ADDER

A carry-save adder is a type of digital adder, used in computer micro architecture to compute the sum of three or more n-bit numbers in binary. It consists of group of stand-alone full Adders.

The n-bit CSA consists of n disjoint full adder where each of which computes a single sum and carry bit based on the corresponding bits of the three input numbers. It consumes three n-bit input integers to be added and produces two outputs, n -bit partial sum and n-bit carry. A carry-save adder consists of multi one-bit full adders without any carry chaining unlike the normal adders such as ripple carry adder.

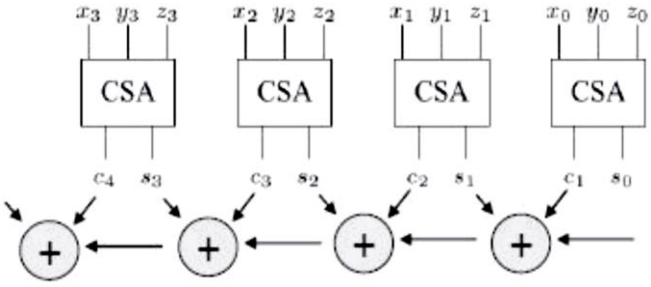

Fig 6: Block Diagram of Carry Save Adder [6]

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IV. PROPOSED DESIGN

16X16 Vedic Multiplier based on Carry Save Adder:

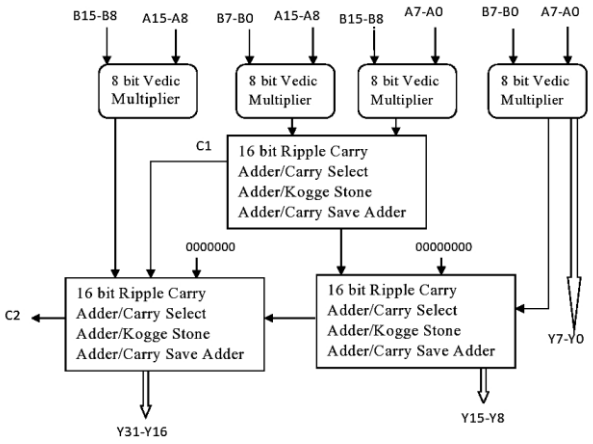

Fig 7: Proposed architecture for 16-bit Vedic multiplier

This is the 16X16 structure of Vedic multiplier based on carry save adder; this multiplier is implemented from the 8X8 multiplier. In this diagram A0 to A15 are the bits of first digit and B0 to B15 are the bits of second digit For 16X16 multiplier, we require four 8X8 multiplier and three carry save adders and after doing the procedure, we will get the result of 16X16 multiplier and the result obtained is of 32 bits. Each input byte is handled by a separate 8×8 Vedic multiplier to produce sixteen partial product rows. These partial products rows are then added in a 16-bit carry save adder optimally to generate final product bits.

Fig [7] the schematic of a 16×16 block designed using 8×8 blocks. The partial products represent the Urdhva vertical and cross product terms.

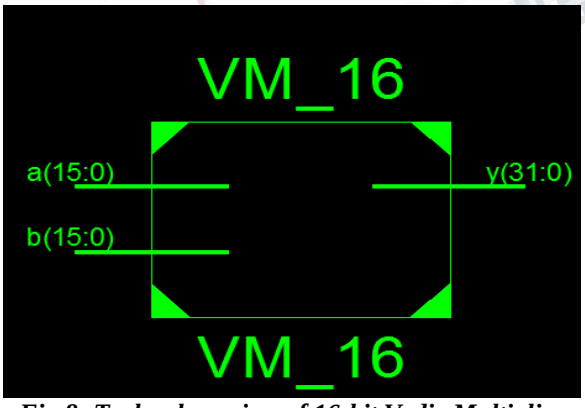

Fig 8: Technology view of 16-bit Vedic Multiplier

Technology view of 16-bit Vedic Multiplier based on carry save adder is shown in Fig [8].

V. RESULTS & DISCUSSIONS

In this paper, the 16X16 Vedic Multiplier using carry save adder is synthesized and simulated and coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language). The Artix-7 family has been used with the XC 7A200T device.

The figure [9] shows the simulation results of the proposed multiplier.

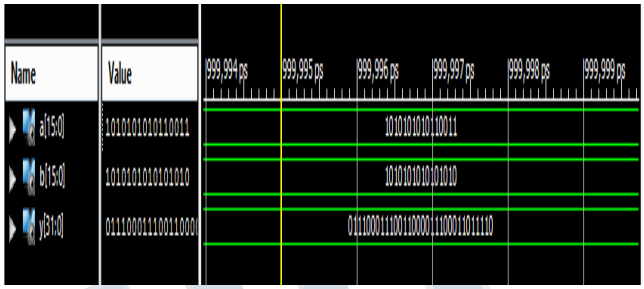

Fig 9: Simulation results of 16 x 16 Vedic multiplier using carry save adder

Vedic Multiplier	Using Modified Carry Select Adder	Using Ripple Carry Adder	Using Kogge Stone Adder	Using Carry Save Adder **(Proposed)**
Maximum Combinational Path Delay (ns)	23.367	48.304	35.732	**13.901**
Peak Memory Usage (MB)	978	1012	998	**835**

Table 1: Comparison of delay and peak memory usage

Table 1 represents the comparison of peak memory usage and maximum combinational path delay for the Vedic multiplier using four adders. The delay of the 16 bit Vedic multiplier using carry save adder is reduced by huge margin of 40.49%, 71.22% and 61.09% over the 16 bit Vedic multiplier using modified carry select adder, ripple carry adder and kogge stone adder respectively. Table 1 also shows that Vedic multiplier based on carry save adder has lower peak memory usage than Vedic multiplier using modified carry select adder, ripple carry adder and kogge stone adder. Table 2 represents the comparison of power, power-delay product and energy-delay product for the Vedic multipliers based on four different adders. The 16 bit Vedic multiplier based on carry save adder uses 49.05%, 56.23% and 53.23% less power as compared to 16 bit Vedic multiplier using carry select adder, ripple carry adder and kogge stone adder respectively.

PDP is the average energy consumed per switching event (Watts * second = Joule) i.e. rate at which power is consumed over time and provides figure of merit to determine quality of a digital gate. Lower energy number means less power to perform a computation at the same frequency and from table 2 it can be seen this:

Vedic Multiplier	Using Modified Carry Select Adder	Using Ripple carry adder	Using Kogge Stone Adder	Using Carry Save Adder **(Proposed)**
Total Power (mW)	142.92	166.38	155.69	**72.81**
Power Delay Product (mJ)	3.339	8.036	5.563	**1.012**
Energy Delay Product (mJ-ms)	0.078	0.388	0.198	**0.014**

Table 2: Power consumption analysis

The PDP of proposed multiplier shows improvement of 69.69%, 87.40% and 81.80% over Vedic multiplier based on modified carry select adder; ripple carry adder and kogge stone adder respectively. Energy-delay product (EDP) is the average energy consumed multiplied by the computation time required and takes into account that one can trade increased delay for lower energy/operation ,is given by product of PDP and gate delay(tp). Table 2 reveals that the proposed 16-bit Vedic multiplier design has lowest energy delay product among Vedic multiplier based on these adders.

VI. CONCLUSION

In this paper, the design and implementation the 16X16 multiplication using carry save adder is done. The comparative study reveals that the proposed high speed and low PDP 16-bit Vedic multiplier design shows a tremendous improvement over the previously reported multipliers. This multiplier shows less power consumption, peak memory usage and delays over the 16 x 16 Vedic multiplier based on modified carry select adder, ripple carry adder and kogge stone adder. Therefore, Vedic Multiplier using carry save adder has an enhanced speed as well as low power consumption. It can be used in the complex designs such as digital signal processors, image processors etc.

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