

Low power 10T SRAM Using Half-VDD Pre-charge and Row-Wise Dynamically Powered Read

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Abstract— In this paper, we are introducing a new 10T static random access memory cell having single ended decoupled read-bit line (RBL) with a 4T read port for low power operation and leakage reduction. An inverter, driven by the complementary data node (QB), connects the RBL to the virtual power rails through a transmission gate during the read operation. RBL increases toward the VDD level for a read-1, and discharges toward the ground level for a read-0. Virtual power rails have the same value of the RBL pre-charging level during the write and the hold mode, and are connected to true supply levels only during the read operation. The RBL is pre-charged at half the cell's supply voltage, and is allowed to charge and discharge according to the stored data bit. Dynamic control of virtual rails substantially reduces the RBL leakage. The proposed 10T cell in a commercial 65 nm technology is 2.47× the size of 6T with $\beta = 2$, provides 2.3× read static noise margin, and reduces the read power dissipation by 50% than that of 6T. The value of RBL leakage is reduced by more than 3 orders of magnitude and (ION/IOFF) is greatly improved compared with the 6T BL leakage. The overall leakage characteristics of 6T and 10T are similar, and competitive performance is achieved.

Keywords: 10T, charge recycling, leakage reduction, low power, pre-charging, single ended (SE) read bit line (RBL), static random access memory (SRAM), virtual rails.

I. INTRODUCTION

The six transistor (6T) SRAM cell is a widely used standard in industry, it has its own limitations. 6T SRAM not only has conflicting read and write requirements, it also has read static noise margin (RSNM) degradation. The most important factors to consider in the design of SRAM in modern nanometer technologies are the: 1) read stability; 2) write stability; 3) cell supply reduction; 4) power dissipation; 5) leakage currents; 6) bitline (BL) ION to IOFF ratio; and 7) variability. Power dissipation has become a first class design constraint as we have hit the utilization wall, and the low power circuit, architecture, and system level techniques are sought out. In addition, the static random access memory (SRAM) is the most important digital macro and its portion on a system-on-chip (SoC) is ever increasing.

With increasing process variations, achieving specific yield is getting difficult, and novel designs and techniques, including read and write assist circuits, are adopted at the cost of area, power dissipation, or speed to improve the read/write stability and increase the number of cells in a single column.

In this paper, we present our half VDD pre-charge and charge recycling technique for low power read operation.

A 4T read port is designed to employ the proposed technique. Read BL (RBL) is charged and discharged through the read port according to the state of stored bit. Read port is powered by virtual power rails that run horizontal and are shared by the cells of a word. The dynamic control of read port power rails reduces the RBL leakage substantially.

II. RELATED WORK

Conventional SRAM designs

An SRAM cell uses the positive feedback of cross-coupled inverters (INVs) to store a single bit of information in a complementary fashion. Access transistors provide the mechanism for the read and write operation. Before every access, column BL pair (BL and BLB) is pre-charged to the supply voltage. For the write operation, one of the pre-charged BLs is discharged through the write driver. SRAM cell must robustly operate under hold, read, and write mode.

The vulnerability of the internal nodes of an SRAM cell is captured through metrics HSNM, RSNM, and WNM/write trip point (WTP) during hold, read, and write mode, respectively.

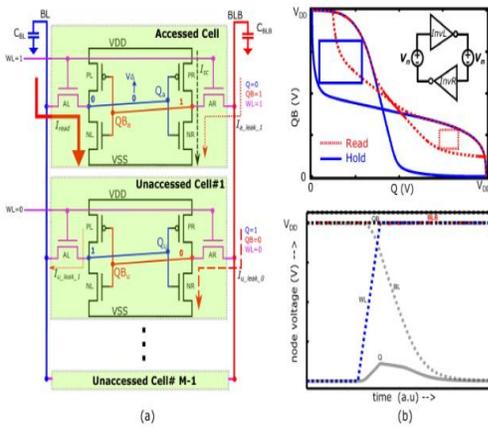


Fig. 1: Conventional 6T SRAM read. (a) Column of M bit-cells during read. (b) Top: hold and read SNM butterfly curve (with worst case noise polarity during hold). Bottom: transient behavior showing read disturbance.

Fig. 1(a) shows a single column of M 6T SRAM cells, where one cell is accessed in read mode with data = 0 ($Q_a = 0$), while other $M - 1$ cells are in the hold mode. Leakage components are labeled, and for the worst case leakage, all $M - 1$ cells store data = 1 ($Q_u = 1$). I-read flows from BL to the VSS through AL and NL of the accessed cell, and the BL voltage is decreased. The unaccessed cell on the BL exhibits BL leakage. I_{uLeak0} is the main component of BL leakage while I_{uLeak1} is negligible, as VDS of AR of the unaccessed cell is large, while VDS of its AL is very small (varies from 0 to VBL). These leakage components decrease the differential BL voltage development.

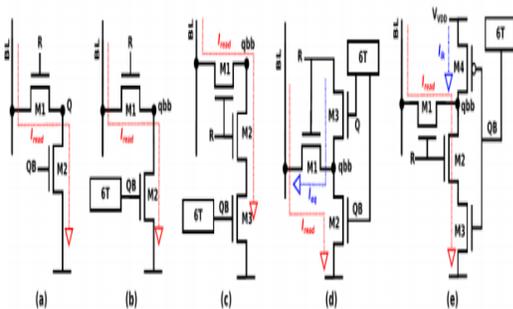


Figure 2: SRAM read ports (a) 6T. (b) 8T. (c) 9T. (d) 9T. (e) 10T.

As there are a large number of cells in a single column, the worst case BL leakage can decrease BLB voltage enough to make an erroneous read. Thus, I-read must be greater than $(M - 1) \times I_{uLeak0}$, where M is the number of cells in a single column.

In essence, 6T SRAM has conflicting read and write requirements and transistor sizing cannot be done independently. Also, 6T has inherit RSNM problem as the read current passes through the cell internal node, and it further degrades with VDD scaling. Also, being considered as baseline design, 6T has overall a higher power dissipation, and higher BL leakages, as the low power techniques employ a certain mechanism to lower the dynamic power dissipation, e.g., charge sharing and hierarchical BL and the leakages (by employing virtual rails).

The read port of 6T SRAM cell is shown in Fig. 2(a) that highlights the internal node Q in the read current path. Many alternative bit cells and techniques have been proposed in the literature to improve SRAM cell stability, reduce the leakage currents, and achieve low power operation compared with the conventional 6T design. An 8T SRAM cell adds a separate 2T read port, shown in Fig. 2(b), and necessarily solves the problem of read stability. Internal nodes are isolated from the read current path, and thus a high RSNM is achieved. Also, sizing of 8T read port can be done independently without affecting the write operation. In 6T SRAM read operation, one of the BL stays at the VDD while the other decreases by VBL amount. However, in the case of 8T SRAM, there is only one BL (RBL) and it either decreases or stays at the VDD level depending on the bit read. Now, the sensing of SE BL can be done using different circuits such as: 1) domino sensing that requires full VDD swing ON the local-BL; 2) pseudo-differential that requires a reference signal; and 3) ac coupled sensing that requires the use of capacitors. Using a reference-based sense amplifier, only a small voltage difference is required.

III. PROPOSED METHODOLOGY

We present our half VDD pre-charge and charge recycling technique for low power read operation. A 4T

read port is designed to employ the proposed technique. Read BL (RBL) is charged and discharged through the read port according to the state of stored bit. Read port is powered by virtual power rails that run horizontal and are shared by the cells of a word. The dynamic control of read port power rails reduces the RBL leakage substantially.

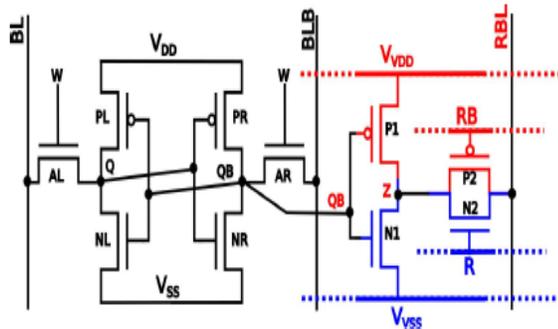


Fig. 3: Proposed 10T SRAM cell with row-wise read port dynamic power lines.

The proposed 10T SRAM cell with SE RBL is shown in Fig. 3. We have added a 4T read port to the 6T cell to decouple the internal nodes during the read operation. Read port consists of an INV P1-N1 driven by node QB, and a transmission gate (TG) P2-N2. The output (Z) of the INV is connected to RBL during the read operation through TG, which is controlled by (read) control signals. Furthermore, read port is powered by virtual power rails, VVDD and VVSS, which are dynamically controlled. These virtual power rails (control signals) run horizontally, and have the true rail values only during the read operation.

- 1) The 10T SRAM cell using an INV and a TG has been proposed earlier. However, our proposed 10T scheme is different from the previous design in the following aspects. The previous INV+TG-based 10T cell was application specific, while our proposed design is generic.
- 2) We have used the dynamically controlled power rails for the read port.
- 3) We pre-charge RBL at VDD/2, while the previous 10T design eliminated the pre-charge phase, and used INV to fully charge or discharge the RBL.
- 4) The basic read technique of both the designs is completely different. The main idea of the proposed design is “the charging or the discharging of the read BL

from VDD/2 for every read operation.” The previous design either discharges from VDD to VSS, or charges from VSS to VDD.

5) A powerful INV was used previously to produce full VDD swing on the RBL. In the proposed design, RBL is pre-charged at VDD/2, and only a small voltage difference (comparable with 6T) is produced for every read cycle.

6) In the proposed design, for every read cycle the RBL will exhibit some change (positive or negative) from its pre-charged value of vdd/2. However, the RBL would not change for consecutive similar bit reads. RBL would change only if consecutive read bits are different.

Precharging and Read Operation

For the read operation, R goes high and RB goes low and thus the TG is activated to connect RBL to the node Z. If QB is 0, then N1 is OFF and P1 connects node Z to the VVDD, which is high for the read operation. Thus, the read current flows from VVDD (having value of vdd) to RBL (which has value of vdd/2) through P1-TG. Hence, the RBL voltage increases toward the vdd level. Now, for a read-0 operation (i.e., QB = 1), P1 is turned OFF and N1 connects node Z to the VVSS, which is low (0 V) during the read operation.

Dynamic Power

There are two virtual rails, and each one is modulated by value VDD/2 from its nominal value of VDD/2 when the read control signal is asserted. VVSS is generated by passing signal “R” through an INV between VSS and VDD/2.

$$P_v = C_{BL} \times V_{DD} \times \frac{1}{16} \times f$$

Leakage Reduction

As RBL is precharged at vdd/2 level, and read signals are not activated (TG is OFF), RBL leakage is reduced substantially due to near zero VDS of TG. Also, the boosted read signals help reduce the leakage currents.

IV. EXPERIMENTAL RESULTS

Total leakage current of all designs is shown on log-scale in Fig. 5. The 8T has a higher total leakage than the 6T and LP10T. Total leakage current of LP10T is slightly

better than 6T due to the better sizing of LP10T. RBL of 8T and LP10T is shown in Fig. 9(b). Dynamic control of power rails of LP10T provides substantial reduction of the IIRBL. Compared with the 8T, RBL leakage of the LP10T is more than 3 orders of magnitude reduced at typical corner and room temperature, and more than 3.3 orders of magnitude reduced on average over all the process corners.

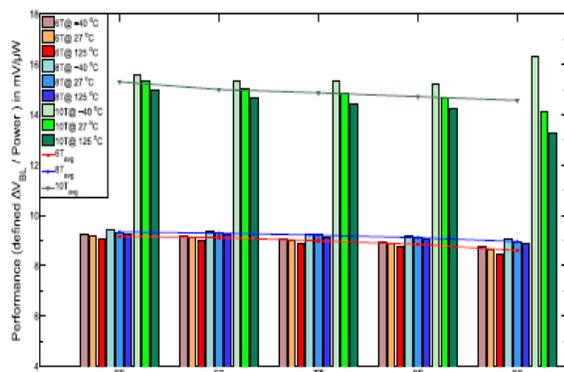


Fig. 4: Performance metric: Pf of 6T, 8T, and LP10T evaluated at different design corners and temperatures. Average Pf of LP10T is $\sim 1.7\times$ that of 6T.

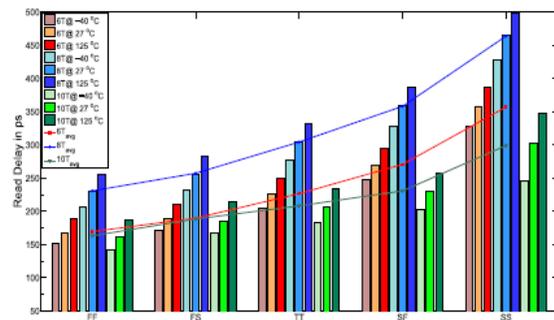


Fig. 5: Read delay (T_{read}) of 6T, 8T, and LP10T evaluated at different process corners and temperatures. LP10T achieves better or competitive speed.

V. CONCLUSION

In this paper, we have presented our 10T SRAM cell that uses a 4T read port and SE RBL. RBL is pre-charged at half the supply voltage and, during the read operation, is charged or discharged according to the bit stored. For a read-0 operation, RBL discharges through

TG and n-MOS transistor, and for the next pre-charge, RBL is supplied current by VP. For a read-1 operation, RBL is charged from $v_{dd}/2$ to v_{dd} by virtual read port. For the next pre-charge, RBL level is decreased and current flows from RBL to VP. By pre-charging through VP (which is half v_{dd}) and charge recycling mechanism, LP10T only dissipates half the average read dynamic power compared with 6T. In 65 nm, performance figure ($mV/\mu W$) of $1.83\times$ of 6T is achieved at 1 V, and $1.84\times$ on average at different supply levels. Due to decoupling of internal nodes, RSNM is increased by $2.3\times$ compared with 6T. Overall leakage power of LP10T is similar to 6T, however, RBL leakage is reduced by more than 3 orders of magnitude, and thus a higher number of cell could be integrated on a single column.

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